

Vegas Schematic

SKL/KBL-U

2016/06/27

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Vegas SKL/KBL-U

Rev

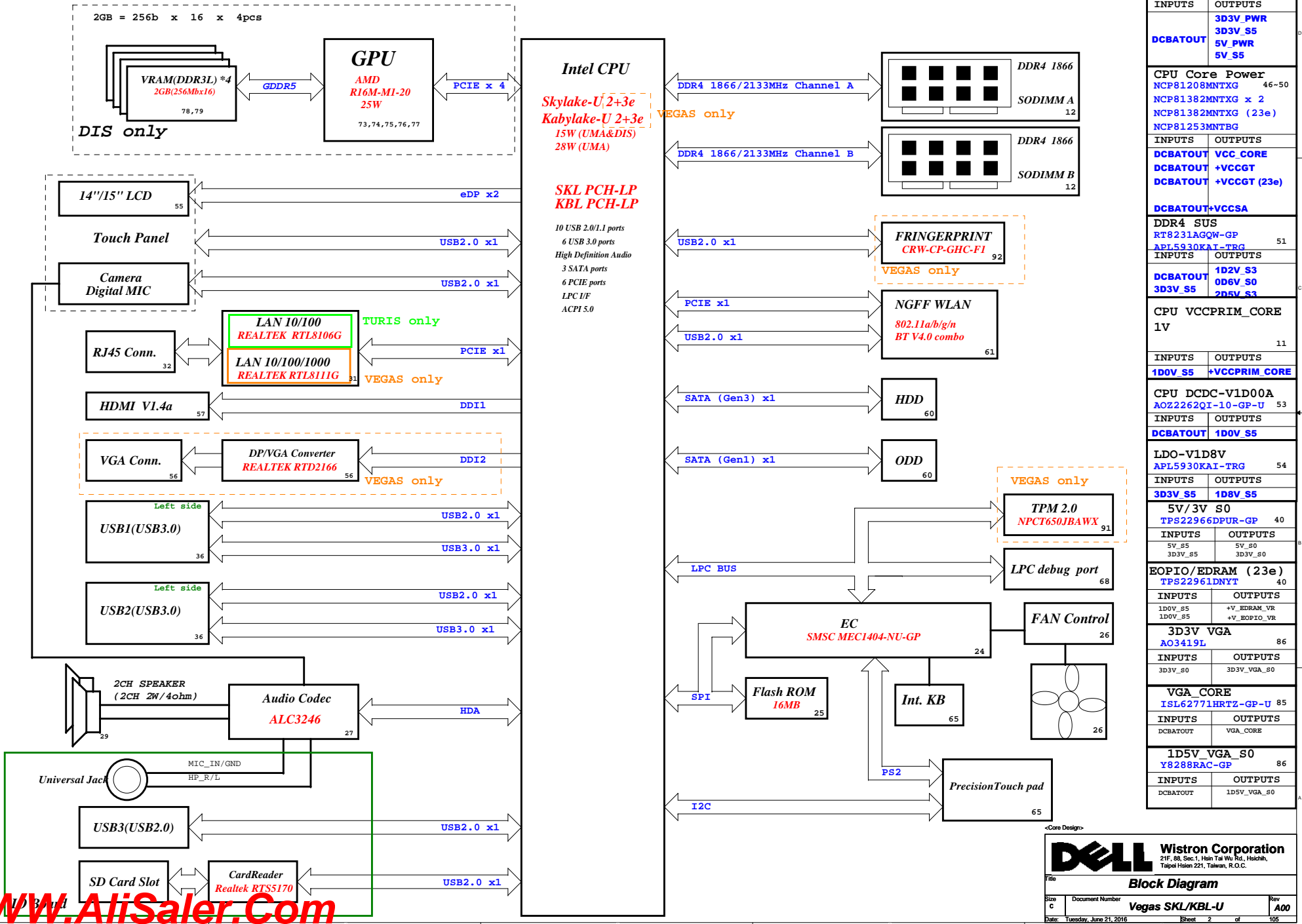
A00

Date: Monday, June 27, 2016

Sheet 1 of 105


Project code:4PD09P010001
PCB P/N: 15341-SD
Revision: A00

Vegas SKL-U/KBL-U Block Diagram



(Blanking)

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Size A4		Document Number Vegas SKL/KBL-U			Rev A00
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Main Func = CPU

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

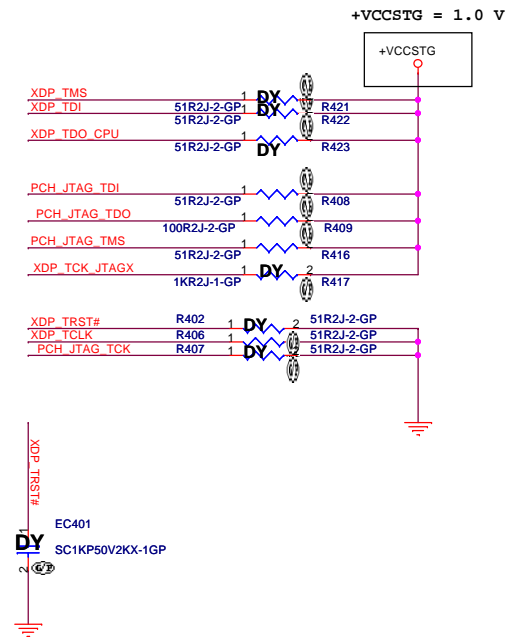
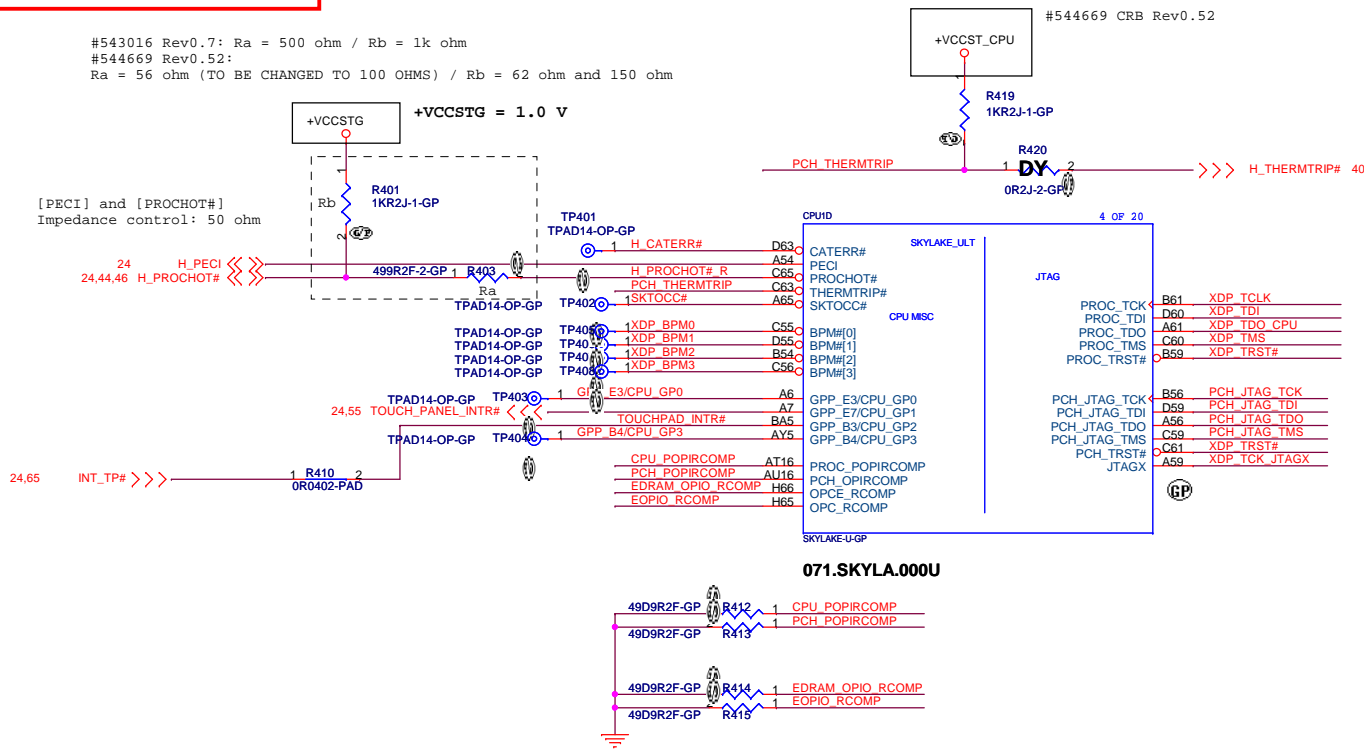
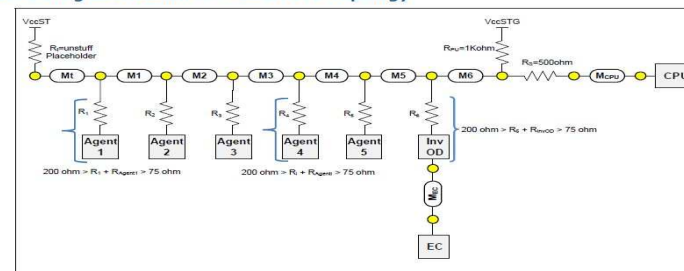


Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

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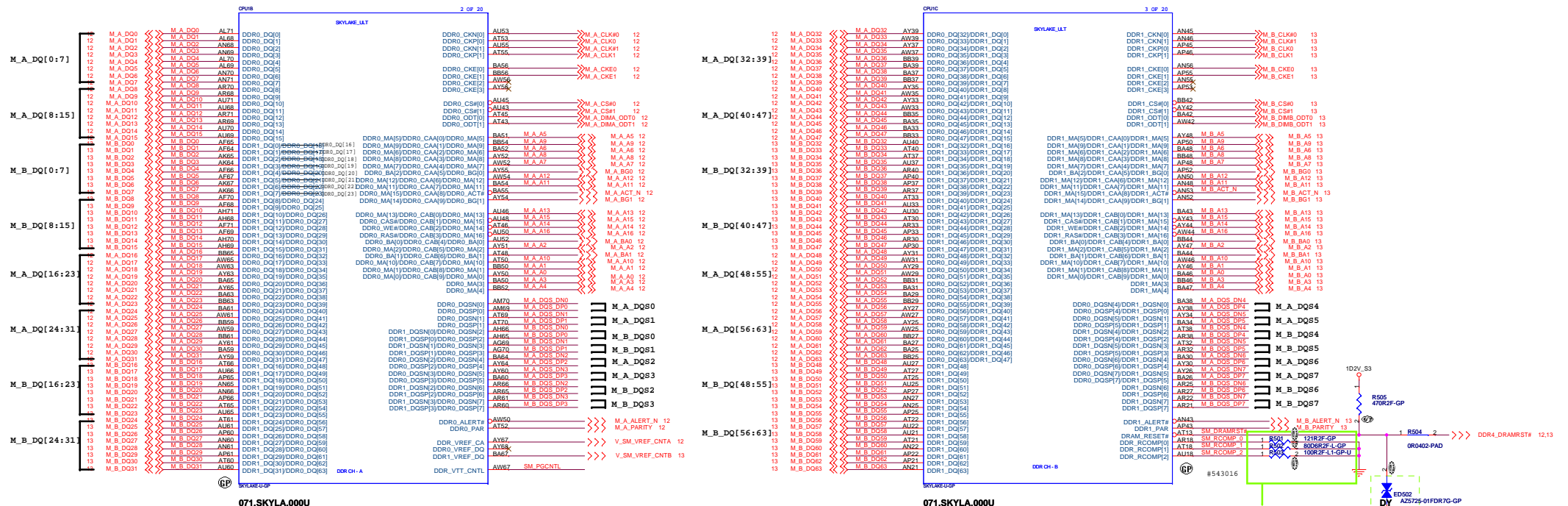


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Title	CPU_ (JTAG/CPU SIDE BAND)
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```
DDR4 ball type: Interleaved Type
```



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLKs) and Strobe (DQS and DQsS) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

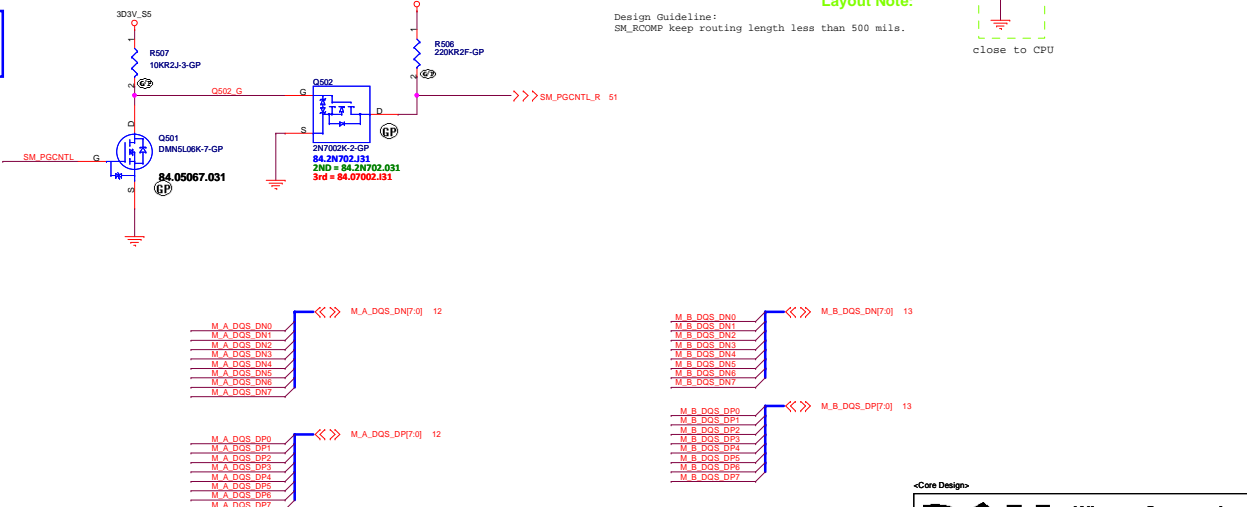
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-7	LPDDR3 Memory Down	Processor	DDIO_DQ[1:0] DDRL1_QD[1:0]	Processor's DQ[1:0] connected to DGRAM's QDT. Fiducialary connection.	1, 2
		DGRAMs	Two DQD per x32 DGRAM INQ Two DQD per x64 DGRAM INQ		
SKL-14	LPDDR3 Memory Down	Processor	DDIO_DQ[1:0] DDRL1_QD[1:0]	Processor's DQ[1:0] connected to DGRAM's QDT. Fiducialary connection.	1, 2
		DGRAMs	One DQD per x32 DGRAM INQ Two DQD per x64 DGRAM INQ	Processor's DQ[1:1] not connected.	
DDR3L Memory Down		Processor	DDIO_DQ[1:1:0] DDRL1_QD[1:1:0]	Processor's DQ[1:0] connected to DGRAM's Rank0 QDT.	3, 4
		DGRAMs	DQ[1:1:0]	Processor's DQ[1:1] connected to DGRAM's Rank1 QDT. If Rank1 is not used, Processor QDT[1:1] not connected.	
DDR3L SO-DIMM		Processor	DDIO_DQ[1:1:0] DDRL1_QD[1:1:0]	Processor's DQ[1:0] connected to DGRAM's QDT.	1, 3
		D12M6s	DQ[1:1:0]		
DDR3L SO-DIMM	Housed Memory SO-DIMM	Processor	DDIO_DQ[1:1:0] DDRL1_QD[1:1:0]	Processor's SDRAM Channel 0's DQ[1:1] connected to DGRAM's Rank0 QDT. Processor's QDT[1:1] not connected.	3, 4
		DGRAMs	DQ[1:1:0]	Processor's DGRAM's Memory Bank0 connected to DGRAM's Rank0 QDT. Processor's QDT[1:1] not connected. DQ[1:1] not connected. DQ[1:1] not connected.	
DDR4 Memory Down		Processor	DDIO_DQ[1:1:0] DDRL1_QD[1:1:0]	Processor's DQ[1:0] connected to DGRAM's Rank0 QDT. Processor's QDT[1:1] connected to DGRAM's Rank1 QDT. Processor's QDT[1:1] not connected.	
		DGRAMs	DQ[1:1:0]		
DDR4 SO-DIMM		Processor	DDIO_DQ[1:1:0] DDRL1_QD[1:1:0]	Processor's DQ[1:1] balls connected to DGRAM QDT[1:1] balls.	
		D12M6s	DQ[1:1:0]		

- Notes:**
- For additional ODT signal connection details see the Customer Reference Board (CRB) schematics and board files (RVP1 - SCL_VLPDR3, RVP5 - SCL_VLPDR3).
 - LPDDR3 Bank0 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
 - DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank0 ODT disable command is enabled RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
- These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 ODP single R16 DDR3L is not supported.



Design Guideline:
SM_RCOMP keep routing length less than 500 miles

Layout Notes

```

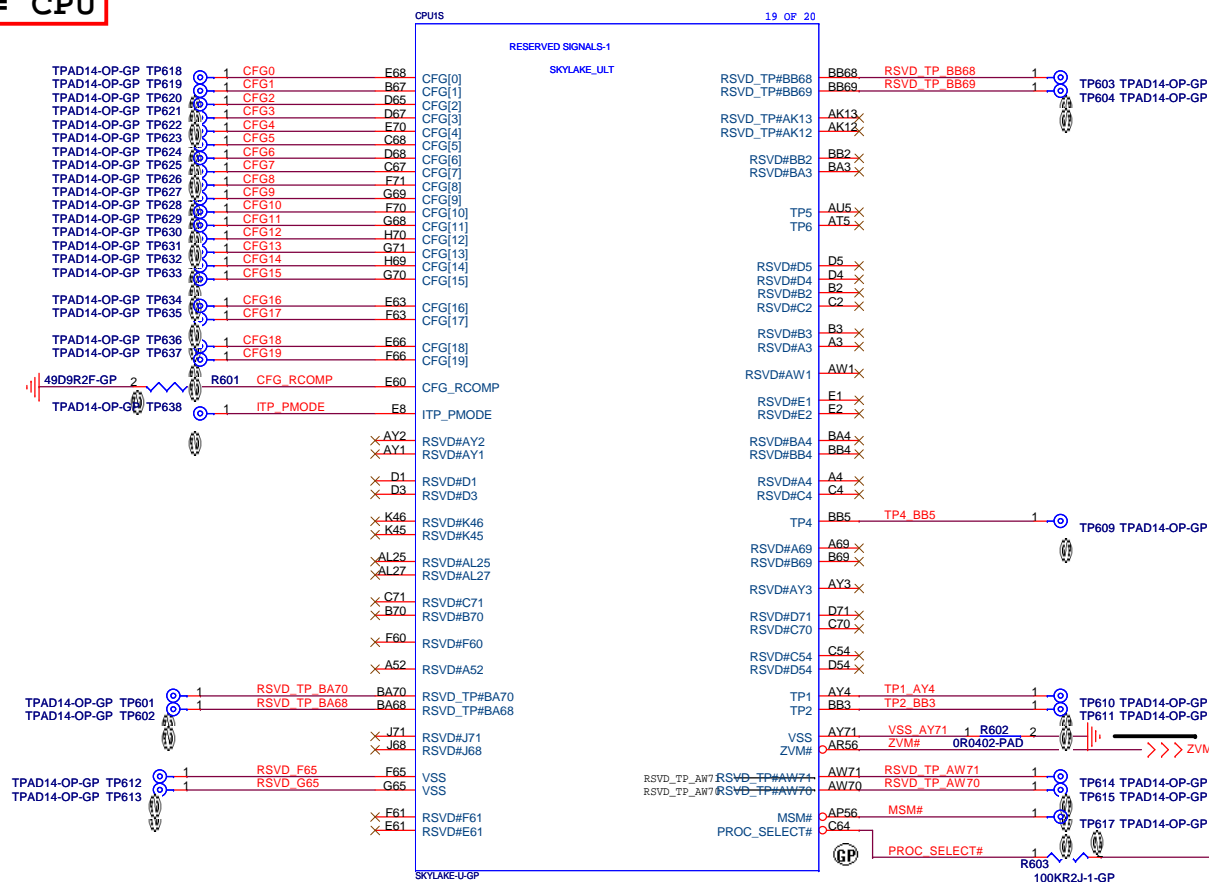
- - - - -
close to CPU

```

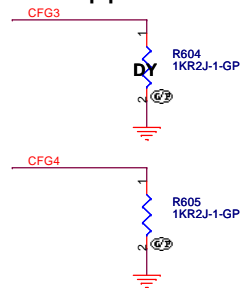
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Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX_ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

#544669 Rev0.52 (CRB)

20140807 david

SKL(#543016):

Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

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Title

CPU (RESERVED)

Size

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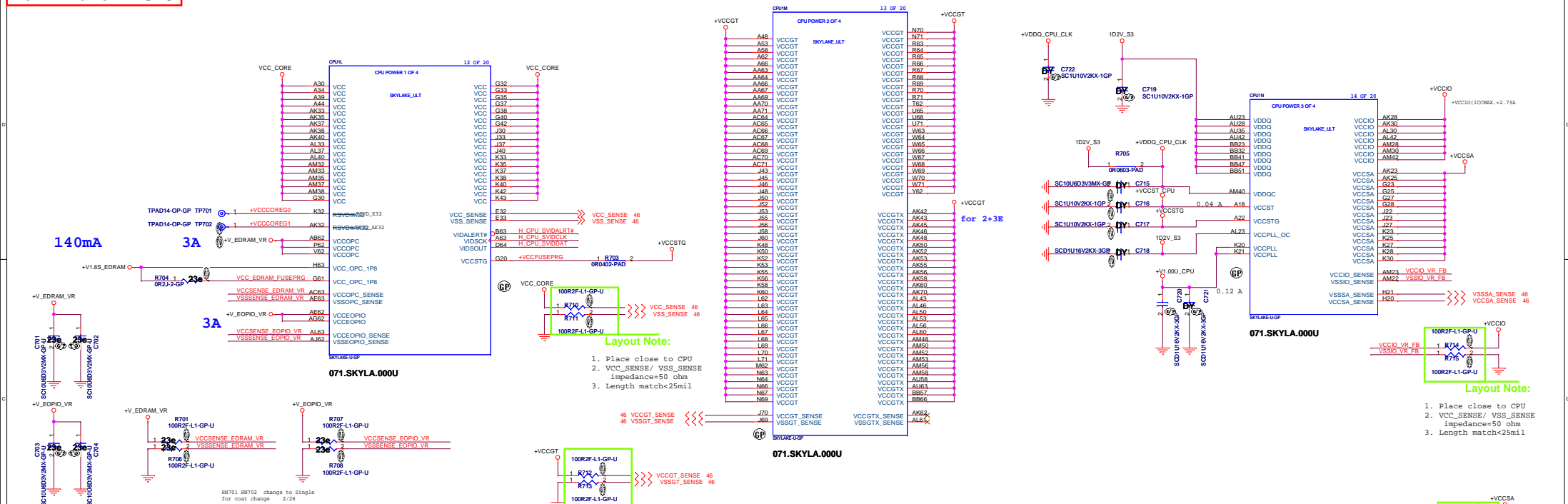
Vegas SKL/KBL-U

Rev	
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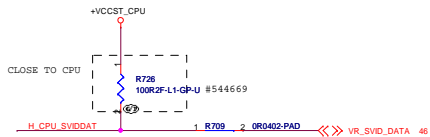
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Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID DATA



SVID CLOCK

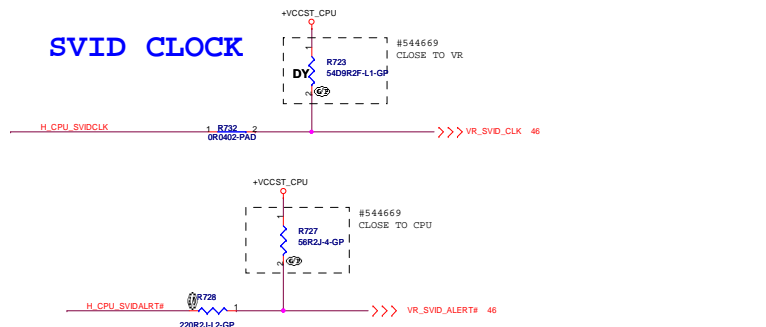
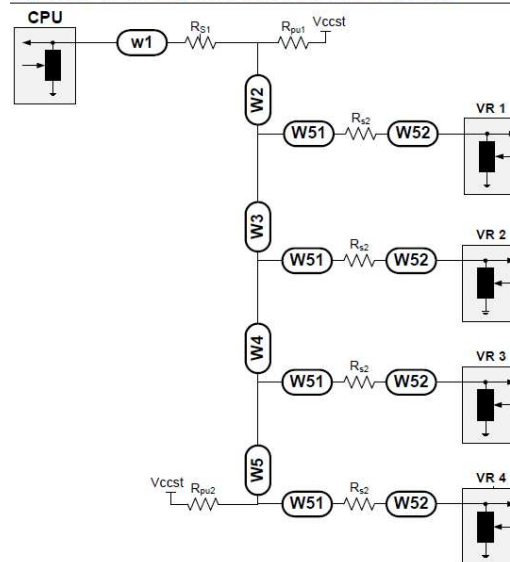


Figure 10-7. Routing Illustration for SVID Topology



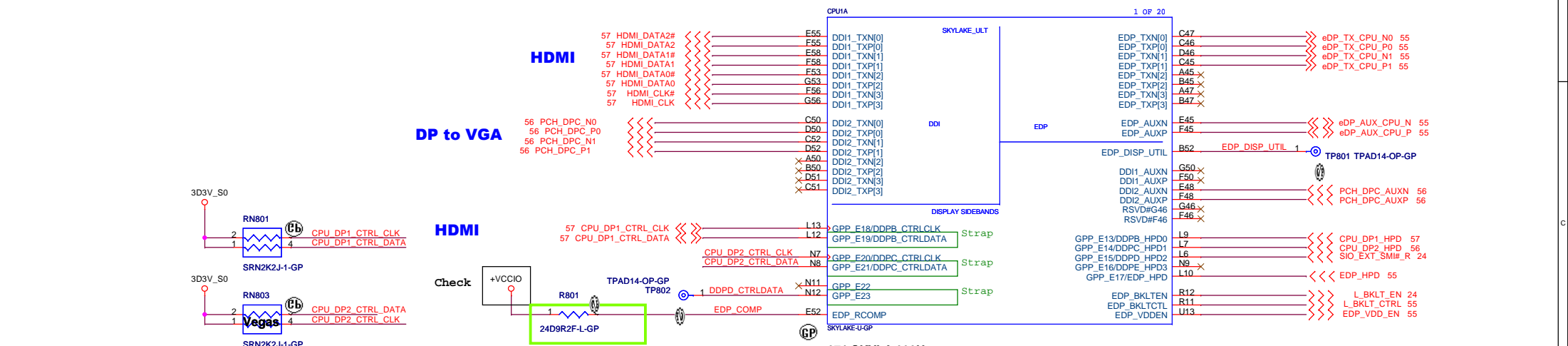
SVID_543016:

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W32 [inches]	R _{OUT} [Ω]	R _{IN} [Ω]	R _S [Ω]	R _L [Ω]	VCC _{PT} [V]
VIDSOUT							100	100	0	10	1.0
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25m1

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071.SKYLA.000U
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

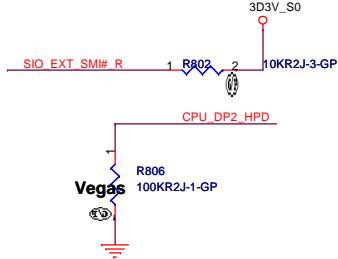
Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 $\pm 1\%$ Ω resistor.



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Title: **CPU (DISPLAY)**

Size: A3 Document Number: **Vegas SKL/KBL-U** Rev: **A00**

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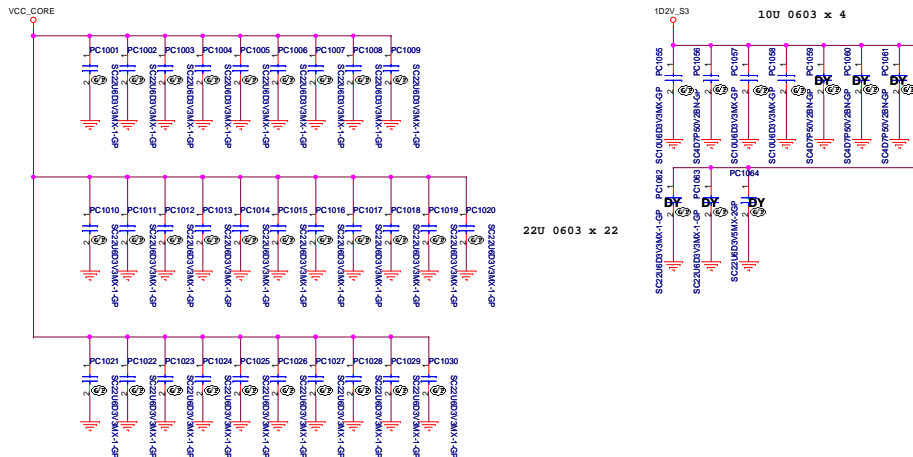
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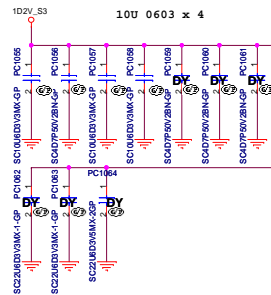
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CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

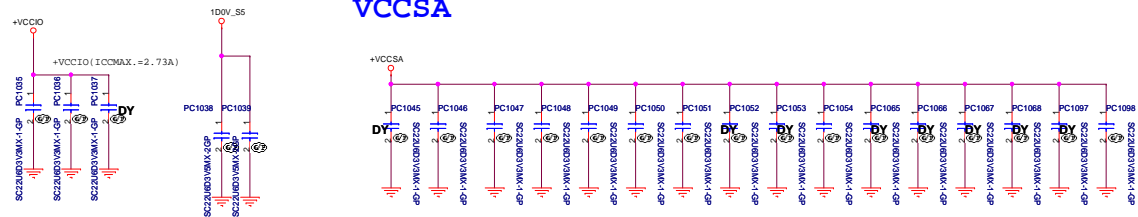


22U 0603 x 22



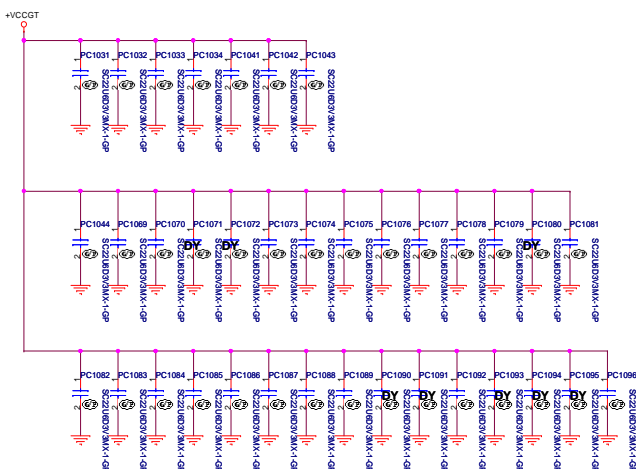
10U 0603 x 4

VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A



22U 0603 x28

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGTx Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCIO Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V) ¹	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V) ¹	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCIOPIO	2x 10uF 0402		Placeholder only
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

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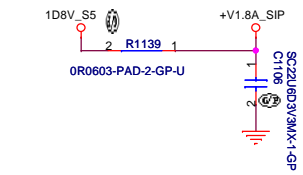
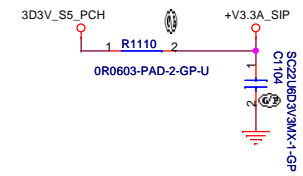
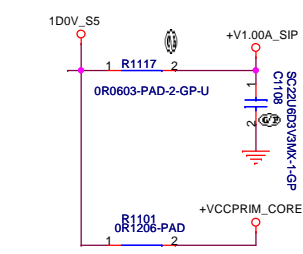
CPU (Power CAP1)

Vegas SKL/KBL-U

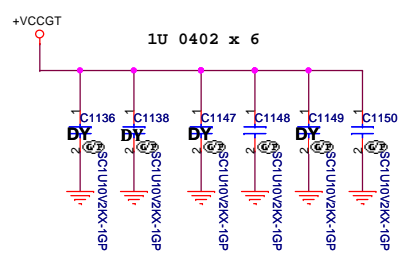
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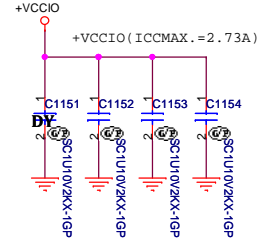
PCH DERIVED RAILS



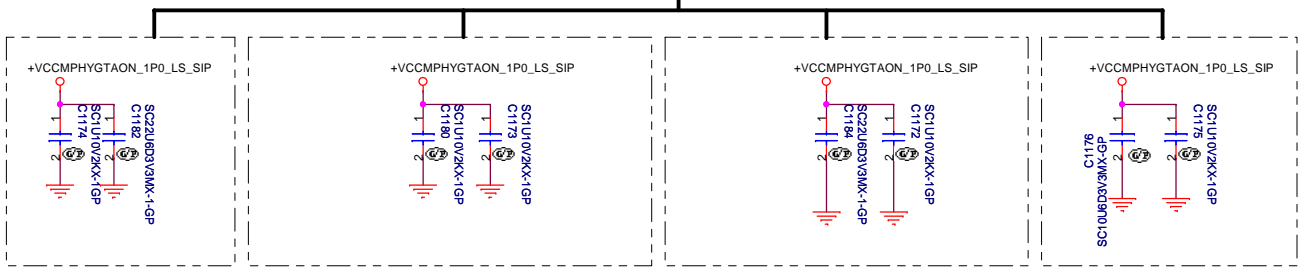
UNSLICED GT



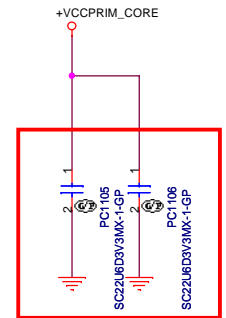
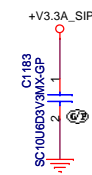
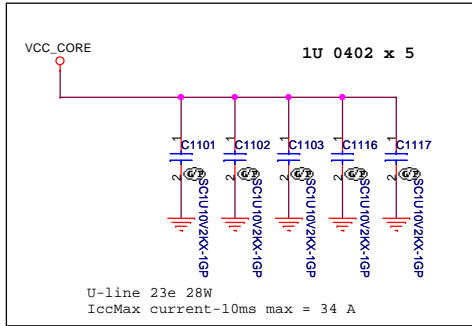
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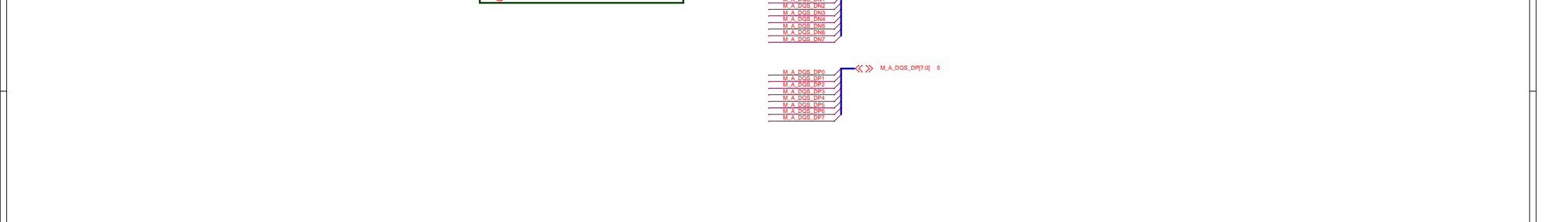
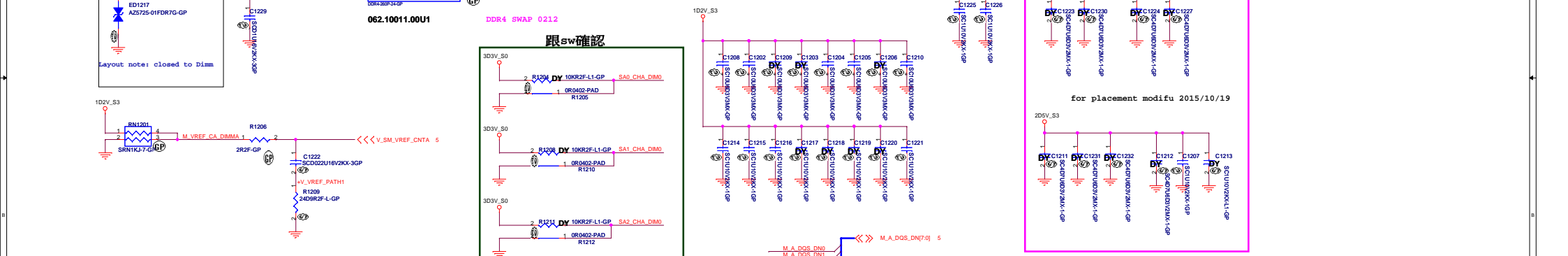
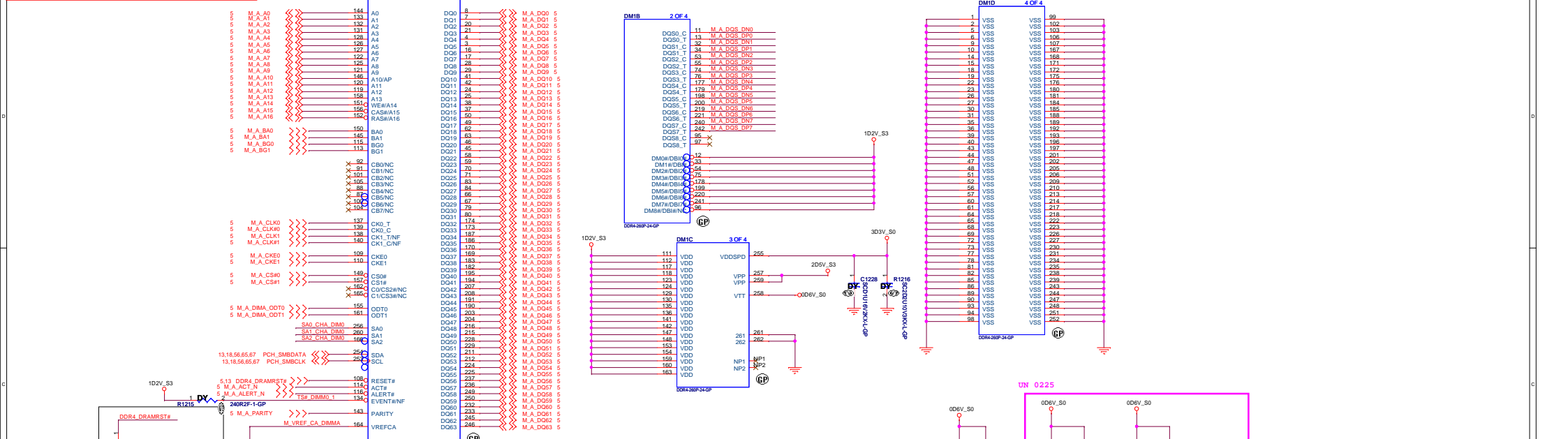


+VCCMPHYGTAON_1P0 (ICCMAX.=2.12A)




Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15





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Title (Reserved)_SODIMM _SODIMM4					
Size A4		Document Number Vegas SKL/KBL-U			Rev A00
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Main Func = PCH

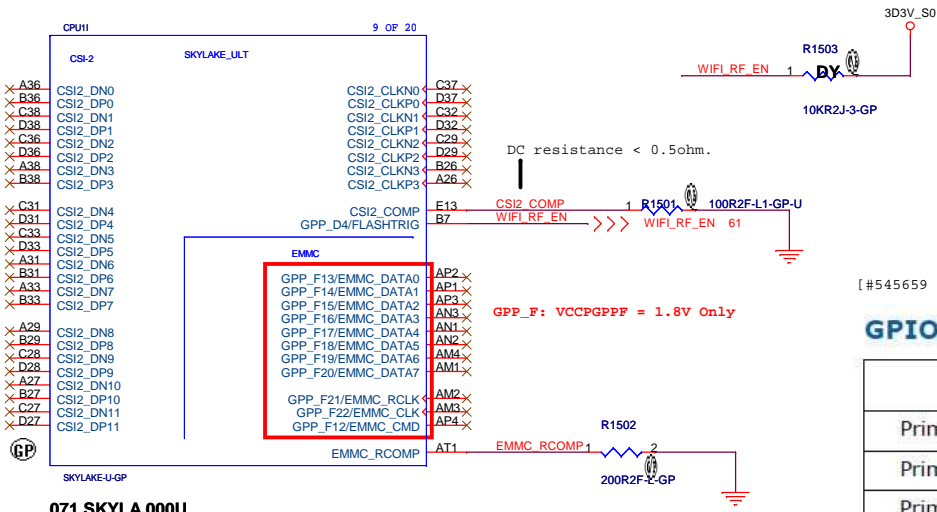


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

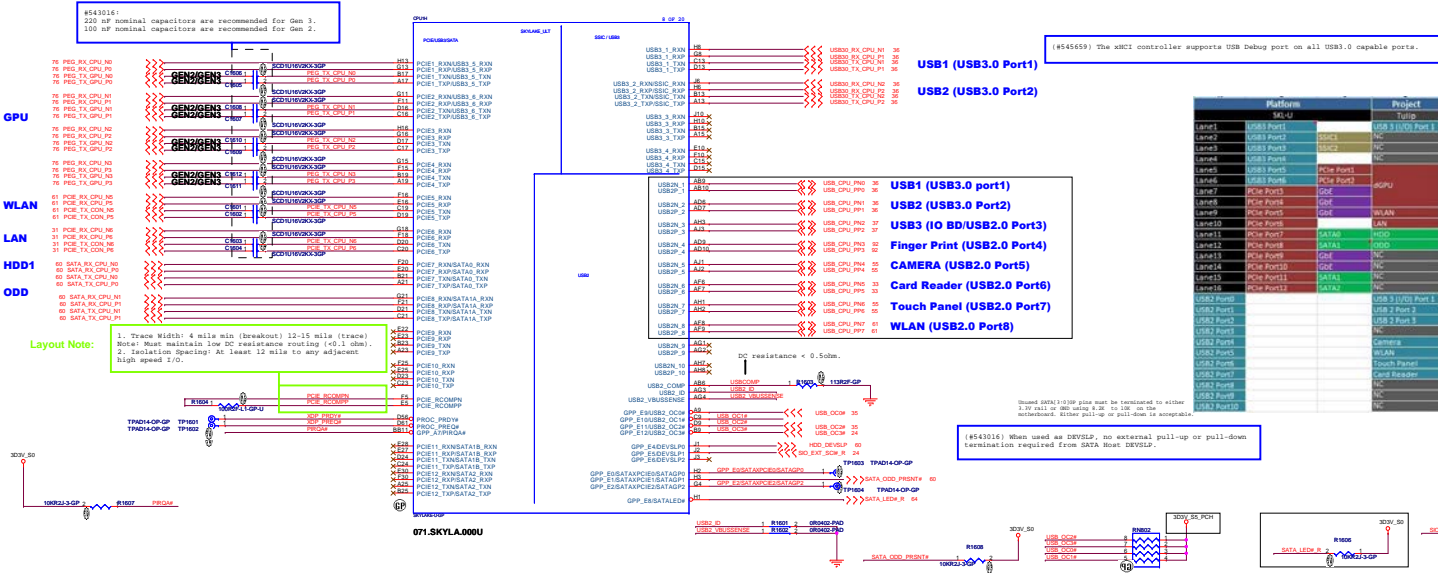
GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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Title			CPU (CS-2/EMMC)	
Size	Document Number	Rev		A00
A3	Vegas SKL/KBL-U			
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	Platform	Project
	SL-U	Tulip
LAN01	USBD Port1	USB 1 (USB Port 1)
LAN02	USBD Port2	NC
LAN03	USBD Port3	USBC
LAN04	USBD Port4	NC
LAN05	USBD Port5	PCIE Port5
LAN06	USBD Port6	PCIE Port6
LAN07	PCIE Port8	GNB
LAN08	PCIE Port9	GNB
LAN09	PCIE Port5	WI-LAN
LAN10	PCIE Port8	LAN
LAN11	PCIE Port7	ATA10
LAN12	PCIE Port8	ATA10
LAN13	PCIE Port9	GNB
LAN14	PCIE Port10	GNB
LAN15	PCIE Port11	ATA11
LAN16	PCIE Port12	ATA11
		USB 1 (USB Port 1)
USBD Port1		USB 2 Port 2
USBD Port2		USB 2 Port 3
USBD Port3		NC
USBD Port4		Camera
USBD Port5		WI-LAN
USBD Port6		Touch Panel
USBD Port7		Cable Reader
USBD Port8		NC
USBD Port9		NC
USBD Port10		NC

PCIe Table			USB 2.0 Table	
Port	Device	Share BUS	Pair	Device
1	N/A	USB3.0_3	0	USB3.0 port1
2	N/A	USB3.0_4	1	USB3.0 port2
3	WLAN		2	USB2.0 Port3 (IOBD)
4	LAN		3	Finger Print
5(L0-L3)	GPU		4	CAMERA
6(L3)	HDD	SATA0	5	Card Reader
6(L2)	ODD	SATA1	6	Touch Panel
6(L0-L1)	N/A		7	WLAN

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

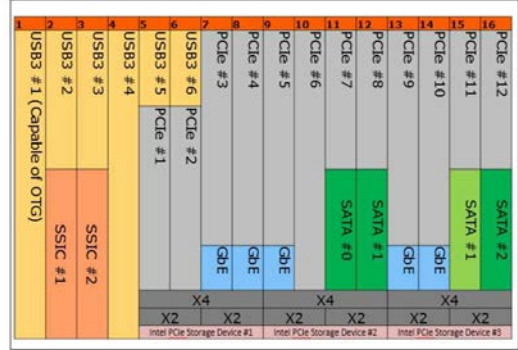


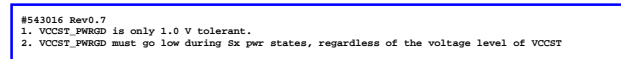
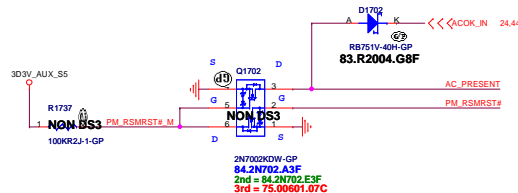
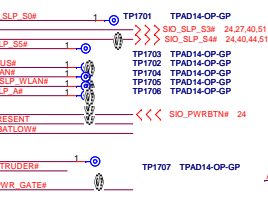
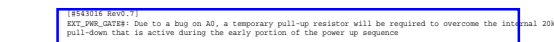
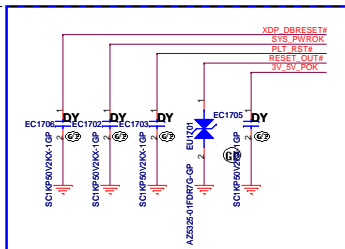
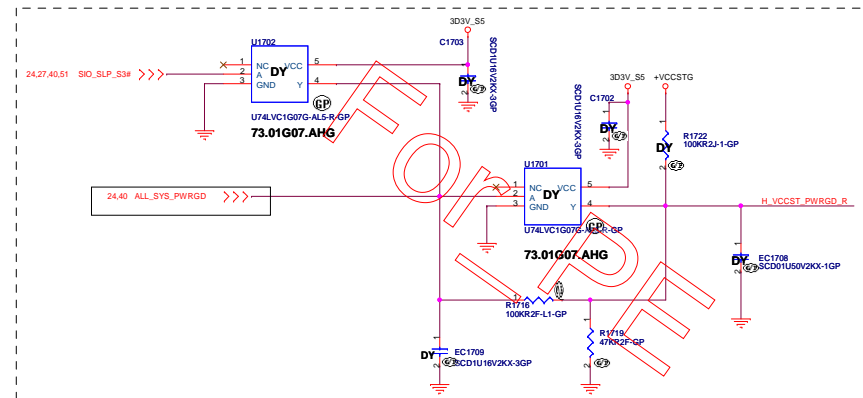
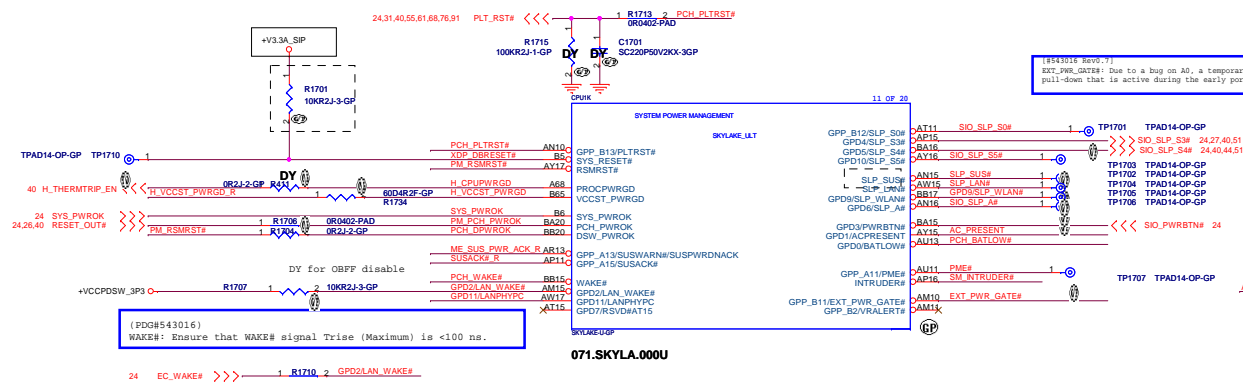
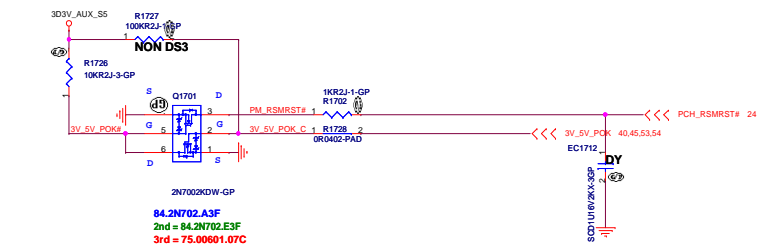
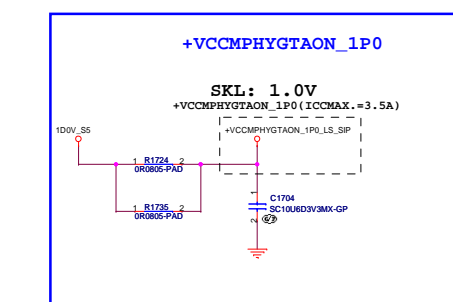
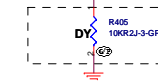
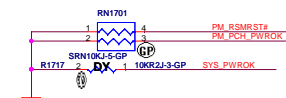
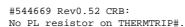
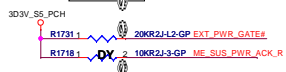
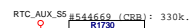
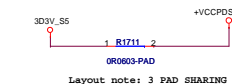
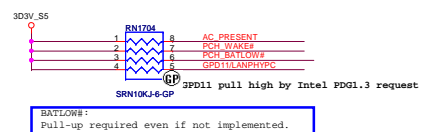
Table 24-2. PCI Express® Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	12b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express® Link Configurations Supported

SKU	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port9		Port12	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x4	Port1				Port5							
Y	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port5		Port7		Port8			
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2												
	2x1									Port9			

Main Func = PCH

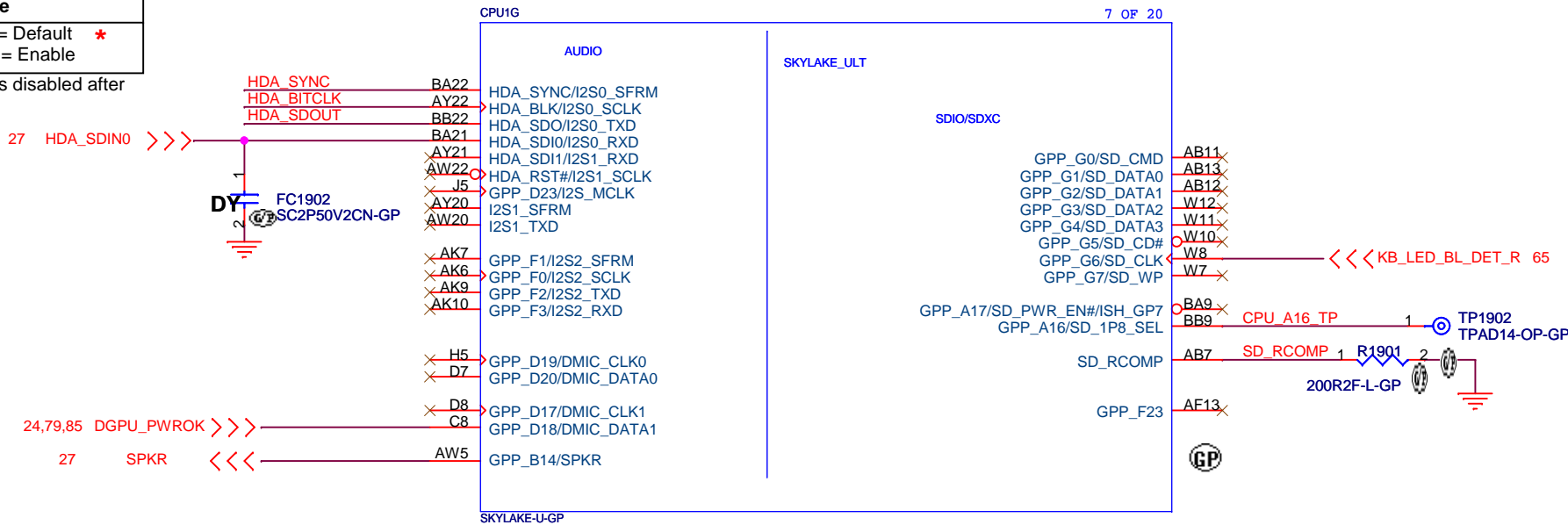


Main Func = PCH

PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after
PLTRST# deasserts

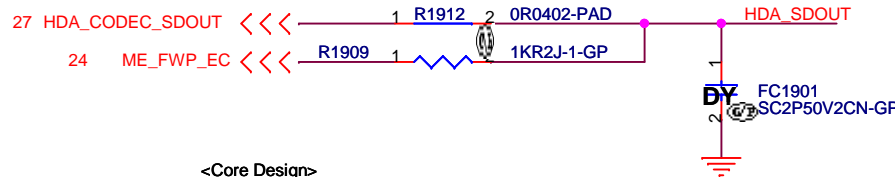
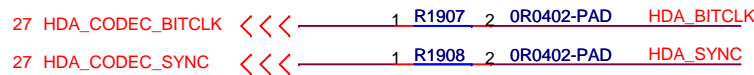
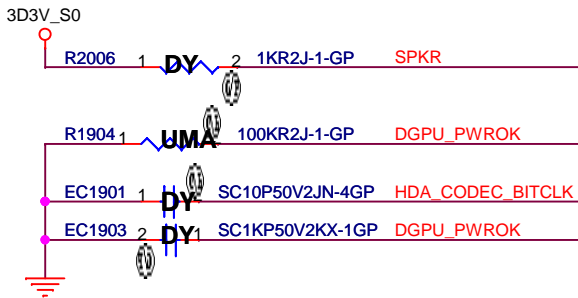


071.SKYLA.000U

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

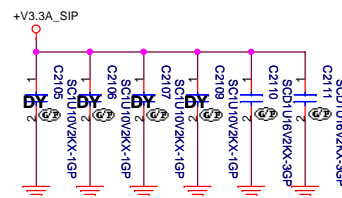
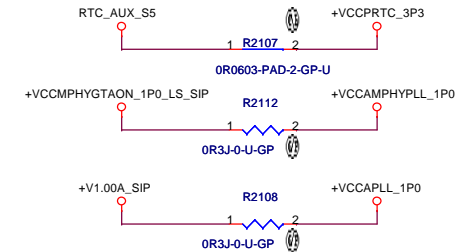
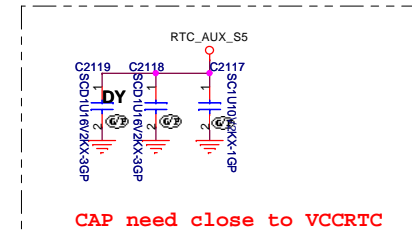
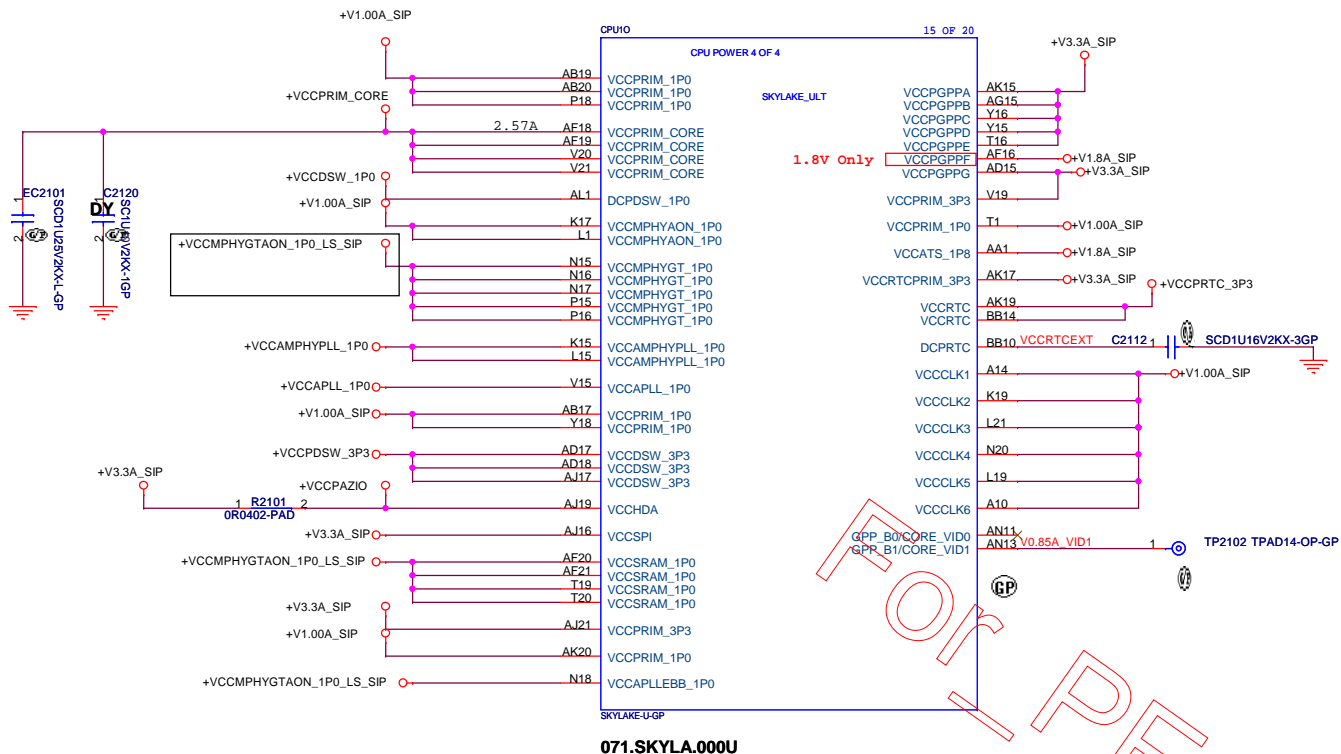
The internal pull-down is disabled after
PLTRST# deasserts



<Core Design>

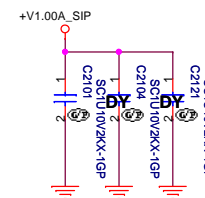
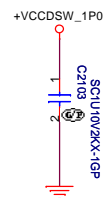
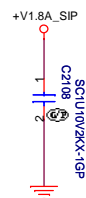
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (AUDIO/SDIO/SDXC)			
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Main Func = PCH



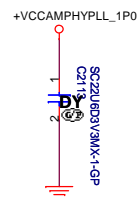
Layout Note:

1uF:
C2105
C2106
C2107
C2109
C2110
C2111



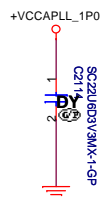
Layout Note:

```
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1
```



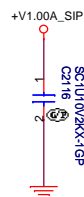
Layout Note:

22uF:



Layout Note:

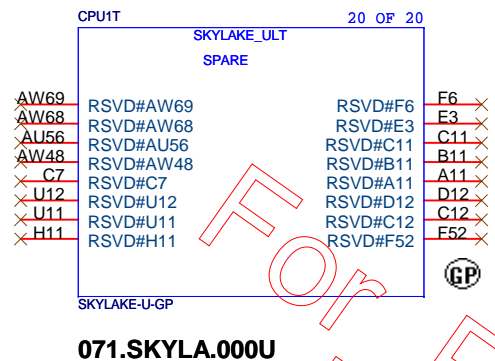
22uF:
C2113




Layout Note:

```
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19
```

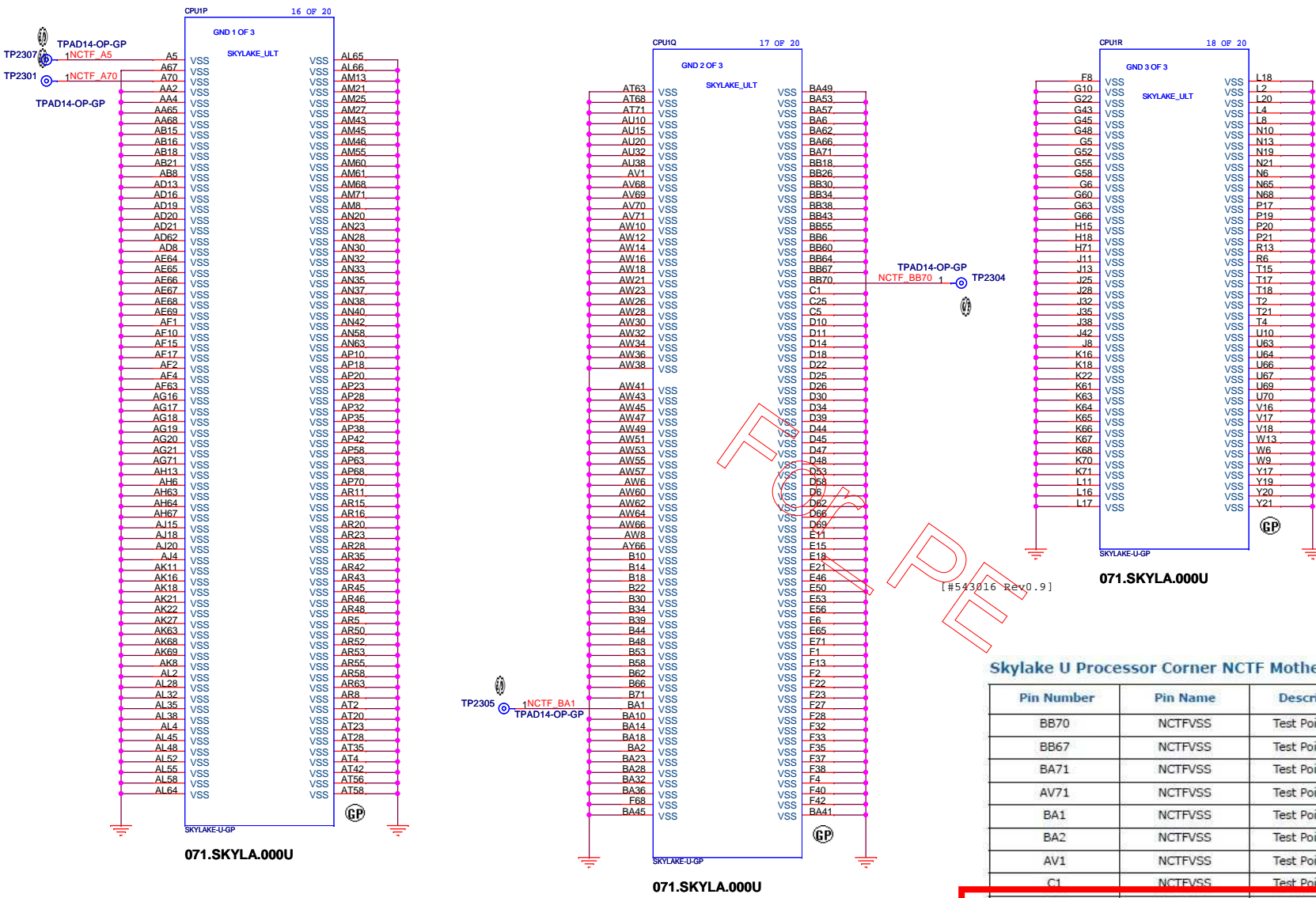

Main Func = PCH



<Core Design>

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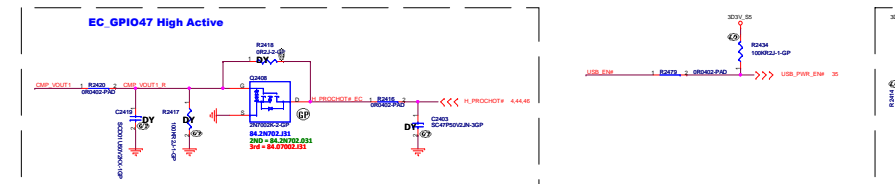
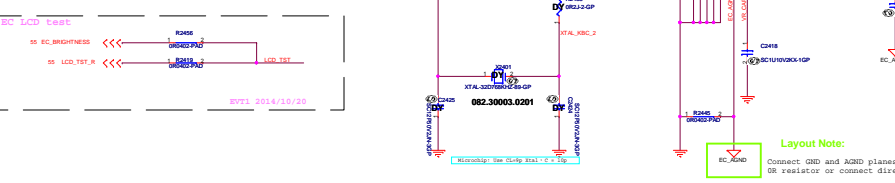
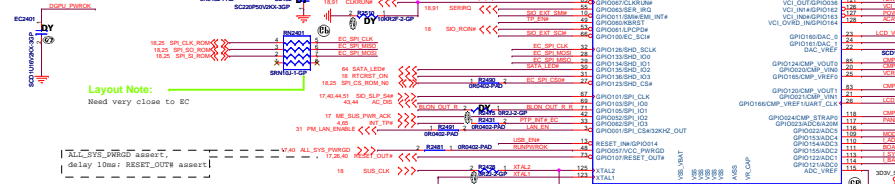
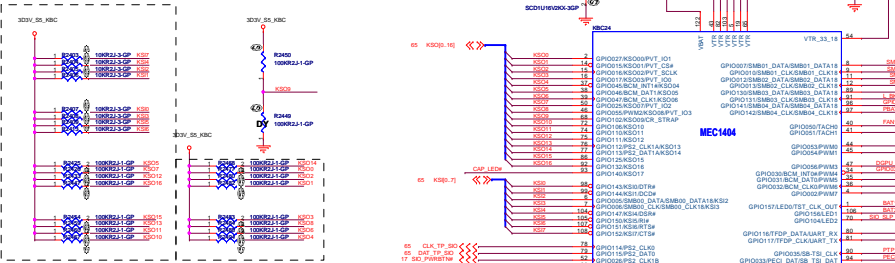
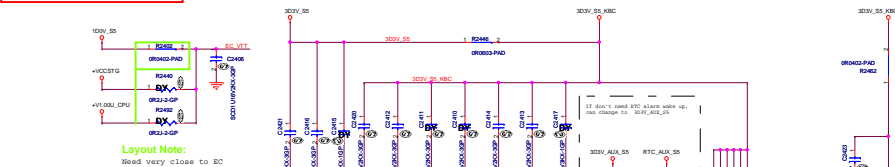
Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

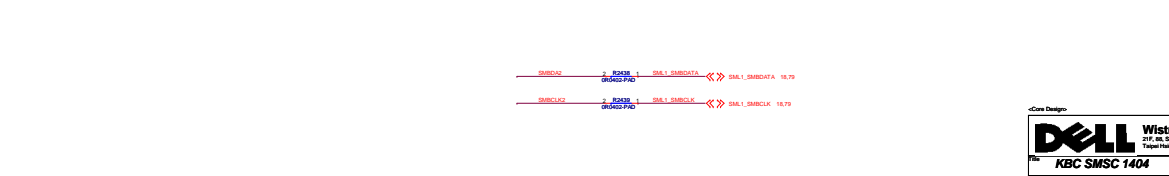
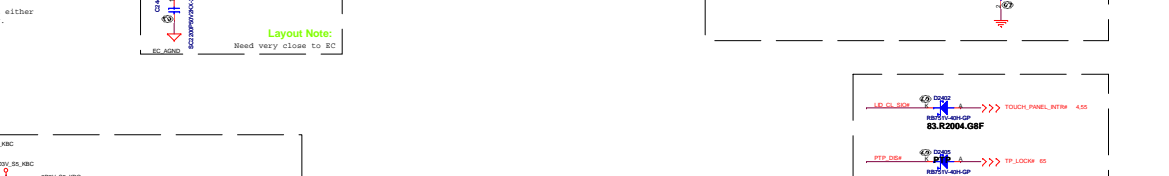
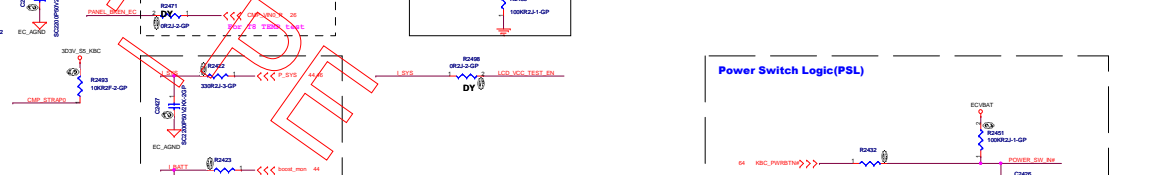
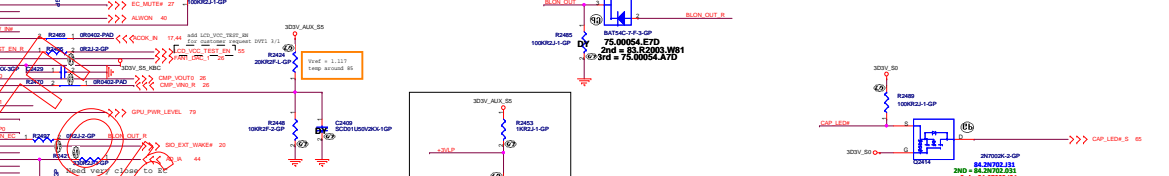
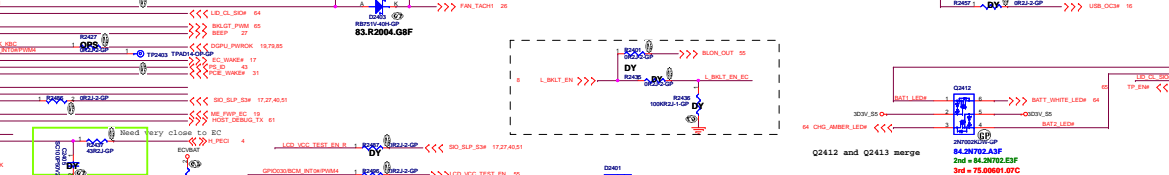
Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Main Func = KBC



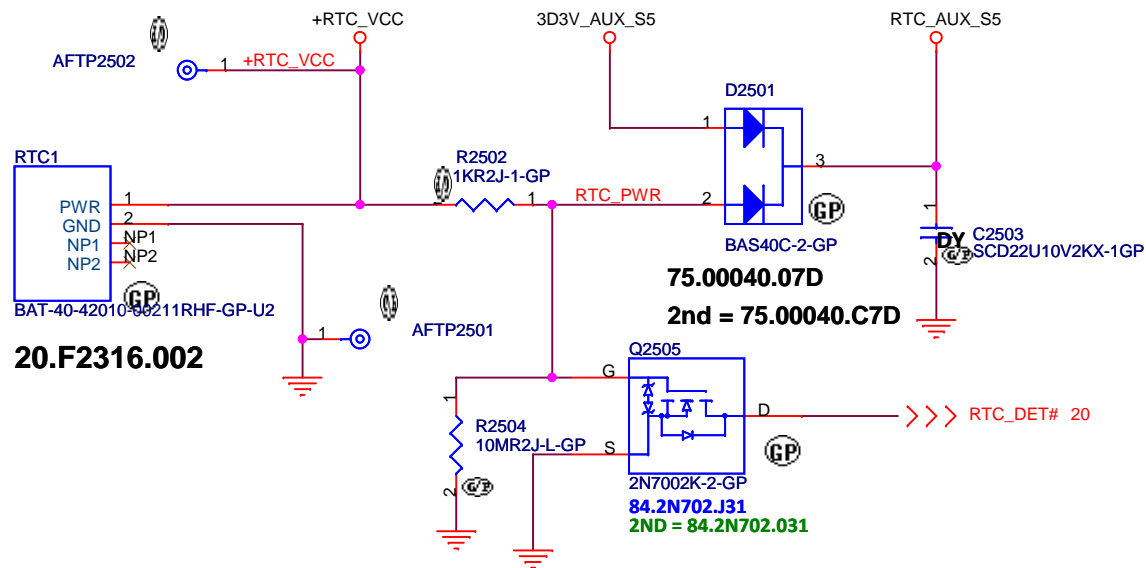
PCB VERSION AD/PINNO	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SR17K1	100.0K	20.0K	2.0V
SR17K2	100.0K	20.0K	2.0V
SR17K3	100.0K	20.0K	2.0V
SR17K4	100.0K	20.0K	2.0V
SR17K5	100.0K	20.0K	2.0V
SR17K6	100.0K	20.0K	2.0V
SR17K7	100.0K	20.0K	2.0V
SR17K8	100.0K	20.0K	2.0V
SR17K9	100.0K	20.0K	2.0V
SR17K10	100.0K	20.0K	2.0V
SR17K11	100.0K	20.0K	2.0V
SR17K12	100.0K	20.0K	2.0V
SR17K13	100.0K	20.0K	2.0V
SR17K14	100.0K	20.0K	2.0V
SR17K15	100.0K	20.0K	2.0V
SR17K16	100.0K	20.0K	2.0V
SR17K17	100.0K	20.0K	2.0V
SR17K18	100.0K	20.0K	2.0V
SR17K19	100.0K	20.0K	2.0V
SR17K20	100.0K	20.0K	2.0V

MODEL_ID DET/GPI07	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SR17K1	100.0K	20.0K	2.0V
SR17K2	100.0K	20.0K	2.0V
SR17K3	100.0K	20.0K	2.0V
SR17K4	100.0K	20.0K	2.0V
SR17K5	100.0K	20.0K	2.0V
SR17K6	100.0K	20.0K	2.0V
SR17K7	100.0K	20.0K	2.0V
SR17K8	100.0K	20.0K	2.0V
SR17K9	100.0K	20.0K	2.0V
SR17K10	100.0K	20.0K	2.0V
SR17K11	100.0K	20.0K	2.0V
SR17K12	100.0K	20.0K	2.0V
SR17K13	100.0K	20.0K	2.0V
SR17K14	100.0K	20.0K	2.0V
SR17K15	100.0K	20.0K	2.0V
SR17K16	100.0K	20.0K	2.0V
SR17K17	100.0K	20.0K	2.0V
SR17K18	100.0K	20.0K	2.0V
SR17K19	100.0K	20.0K	2.0V
SR17K20	100.0K	20.0K	2.0V

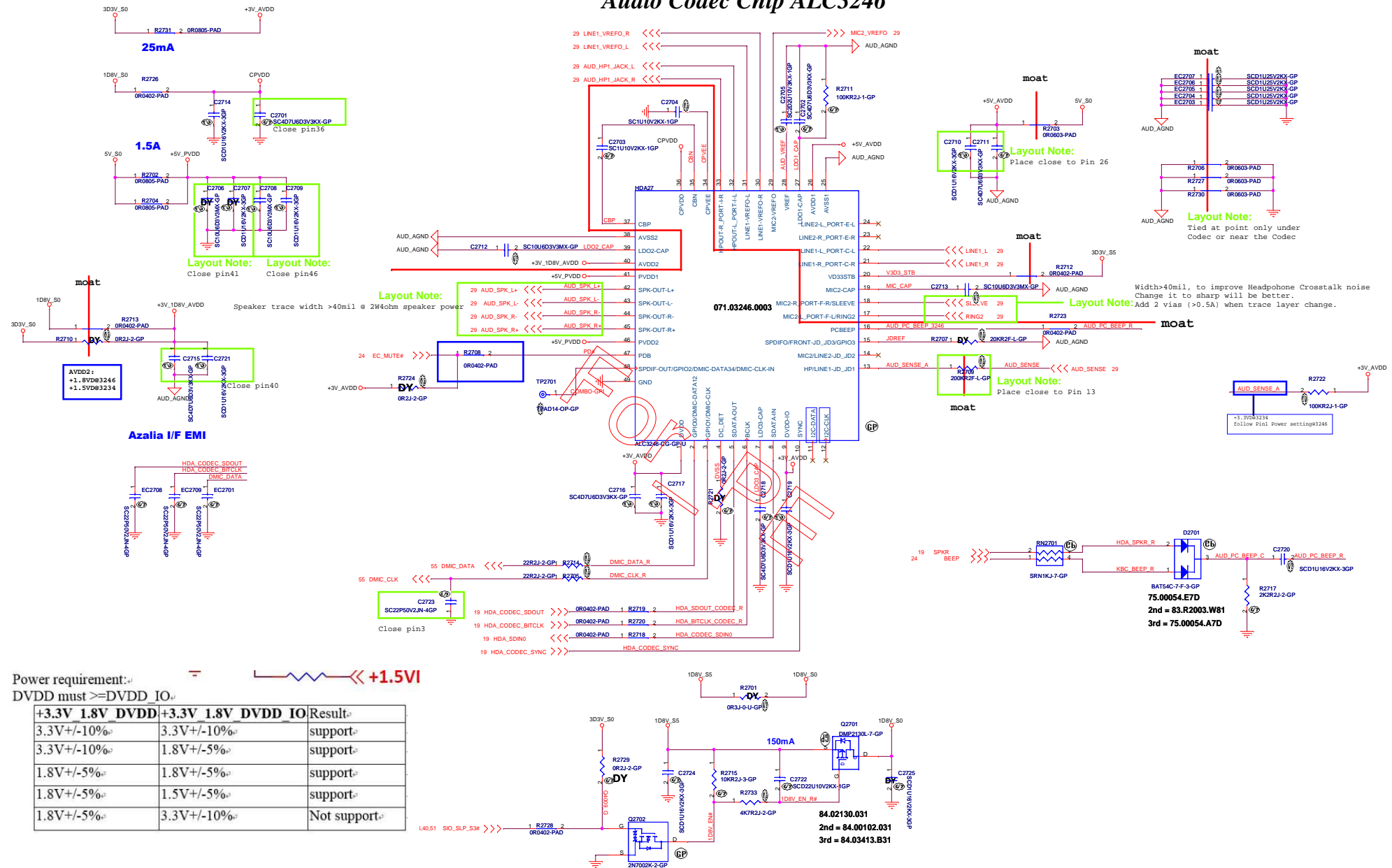


WWW.AliSaler.Com

Main Func = RTC



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+3.3V 1.8V DVDD	+3.3V 1.8V DVDD IO	Result ^o
3.3V+/-10% ^o	3.3V+/-10% ^o	support ^o
3.3V+/-10% ^o	1.8V+/-5% ^o	support ^o
1.8V+/-5% ^o	1.8V+/-5% ^o	support ^o
1.8V+/-5% ^o	1.5V+/-5% ^o	support ^o
1.8V+/-5% ^o	3.3V+/-10% ^o	Not support ^o

(Blanking)

FOR PFE

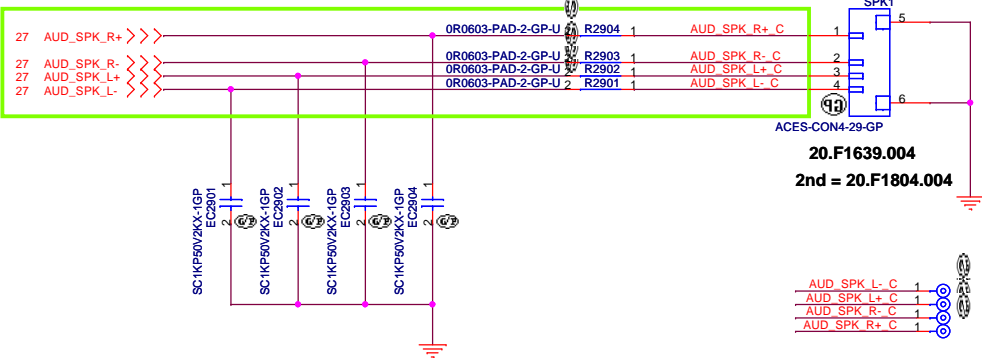
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Main Func = Audio

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

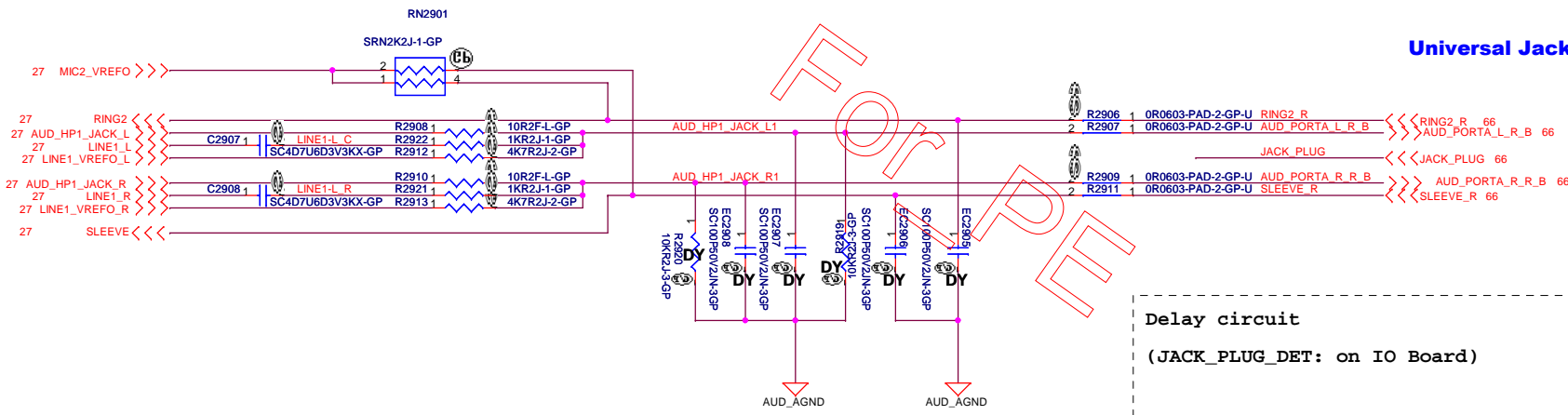


Speaker

SPK1
5
2
4
6
ACES-CON4-29-GP
20.F1639.004
2nd = 20.F1804.004

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

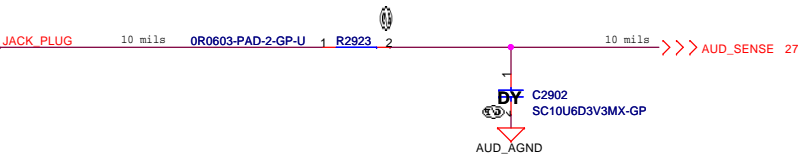
AUD_SPK_L- C 1 AFTP2901
AUD_SPK_L+ C 1 AFTP2902
AUD_SPK_R- C 1 AFTP2903
AUD_SPK_R+ C 1 AFTP2904



Universal Jack (Moved to I/O Board)

Delay circuit

(JACK_PLUG_DET: on IO Board)



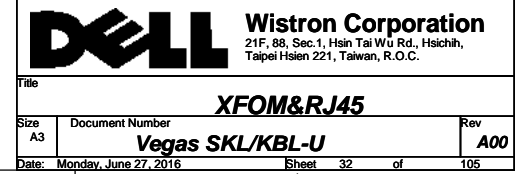
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FOR PE

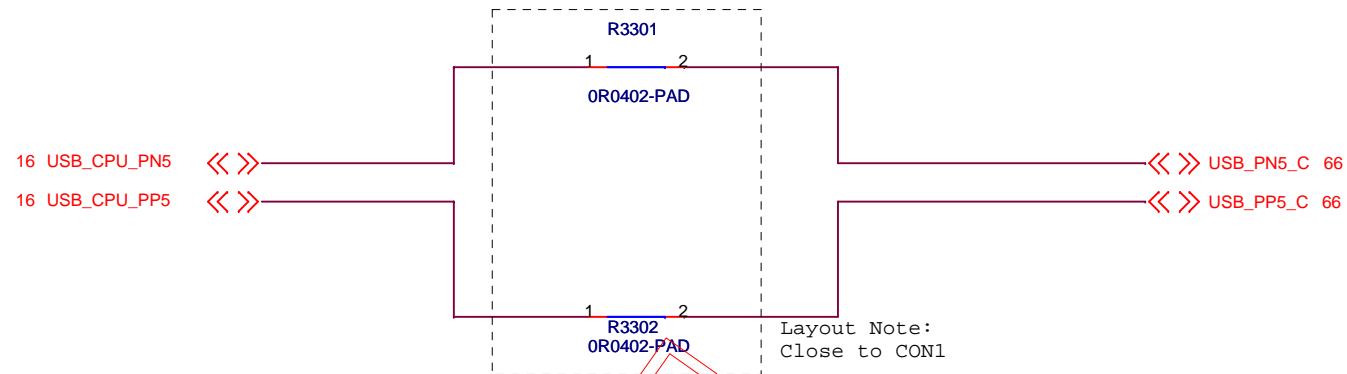
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<Core Design>



Main Func = Card Reader



<Core Design>



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Title

Card Reader-RTS5170

Size
A4

Document Number

Vegas SKL/KBL-U

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A00

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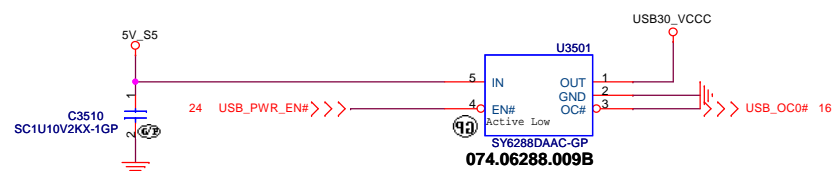
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FOR PFE

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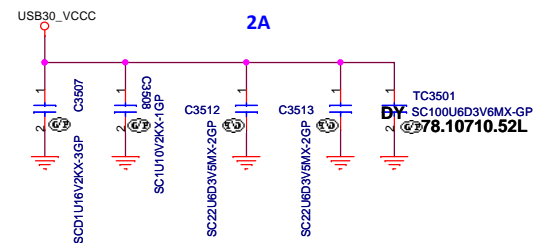
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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = USB3.0 Port1

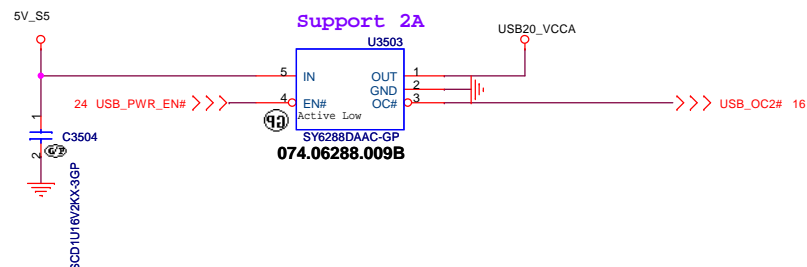


USB3.0 Port1

Layout Note: Close USB1

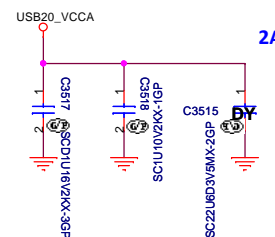


Main Func = USB2.0 Port3

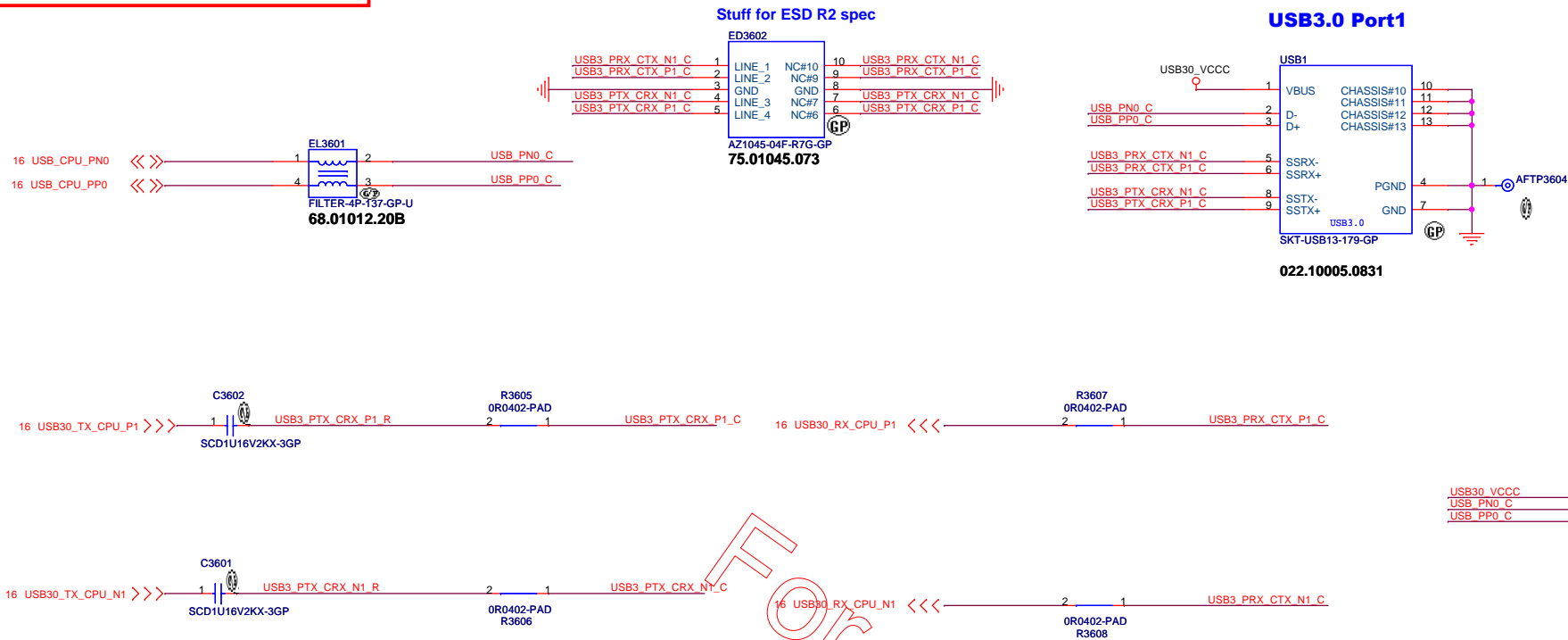


USB2.0 Port3 (IO Board)

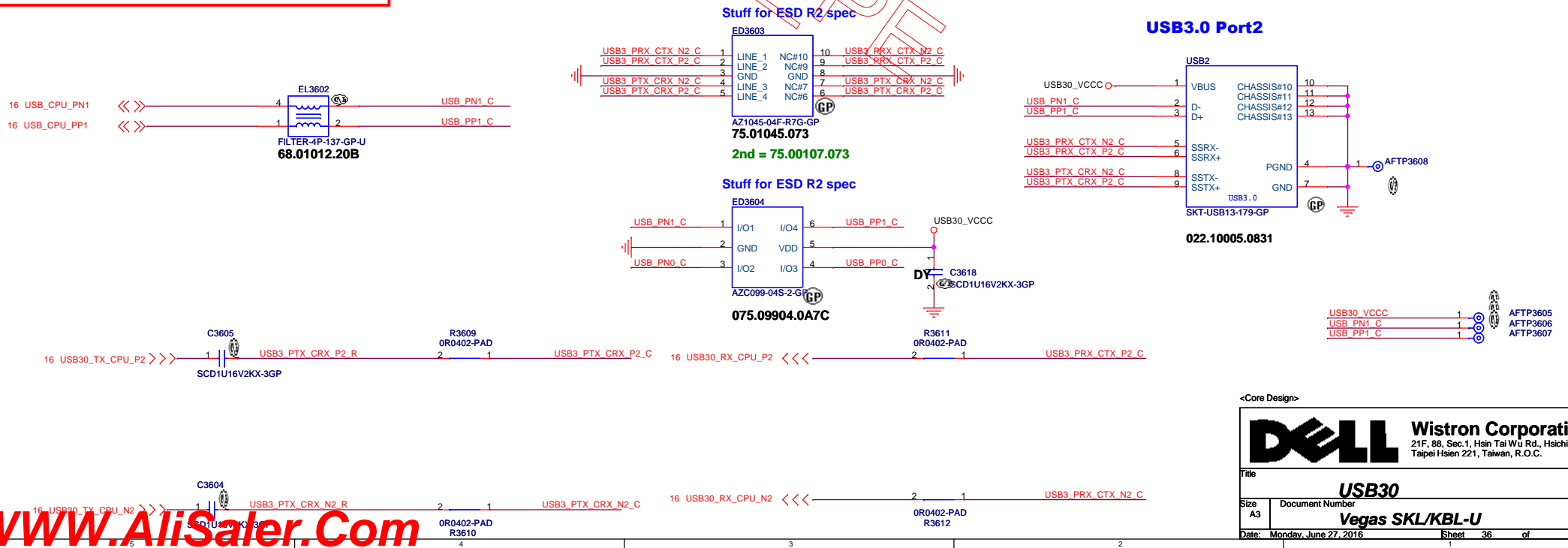
Layout Note: Close CON1



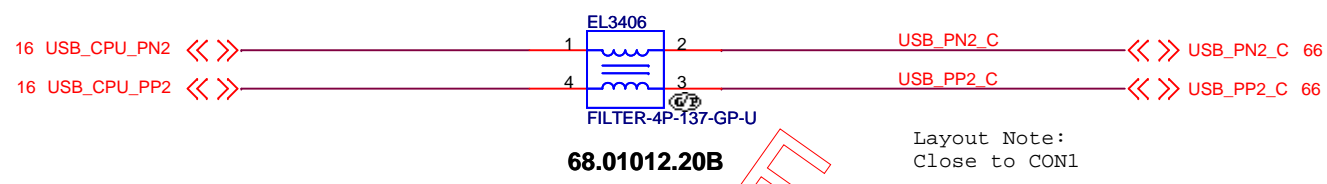
Main Func = USB3.0 Port1



Main Func = USB3.0 Port2

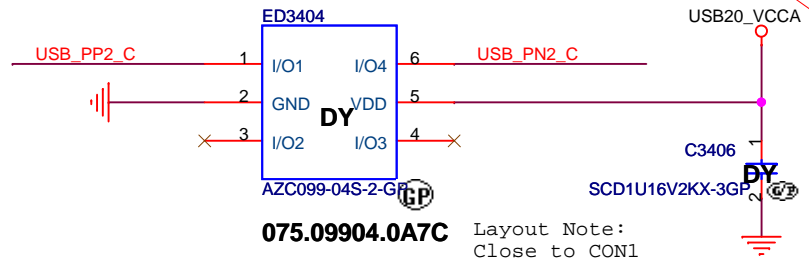


USB port 3 (USB2.0 only) CMC



USB ESD Diode

Stuff for ESD R2 spec




<Core Design>

(Blanking)

For PE


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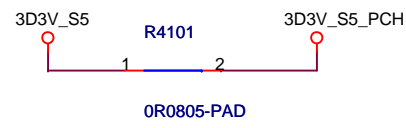
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Main Func = Power & Sequence



For PE

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Title			Connected_Standby(1/2)+DS3		
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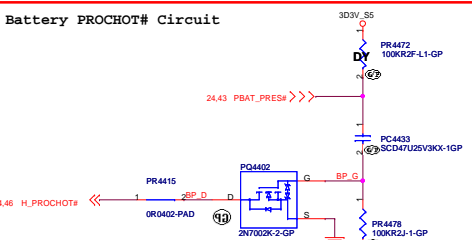
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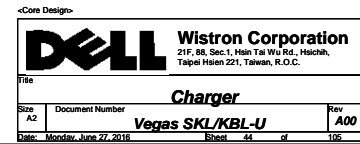
For PE

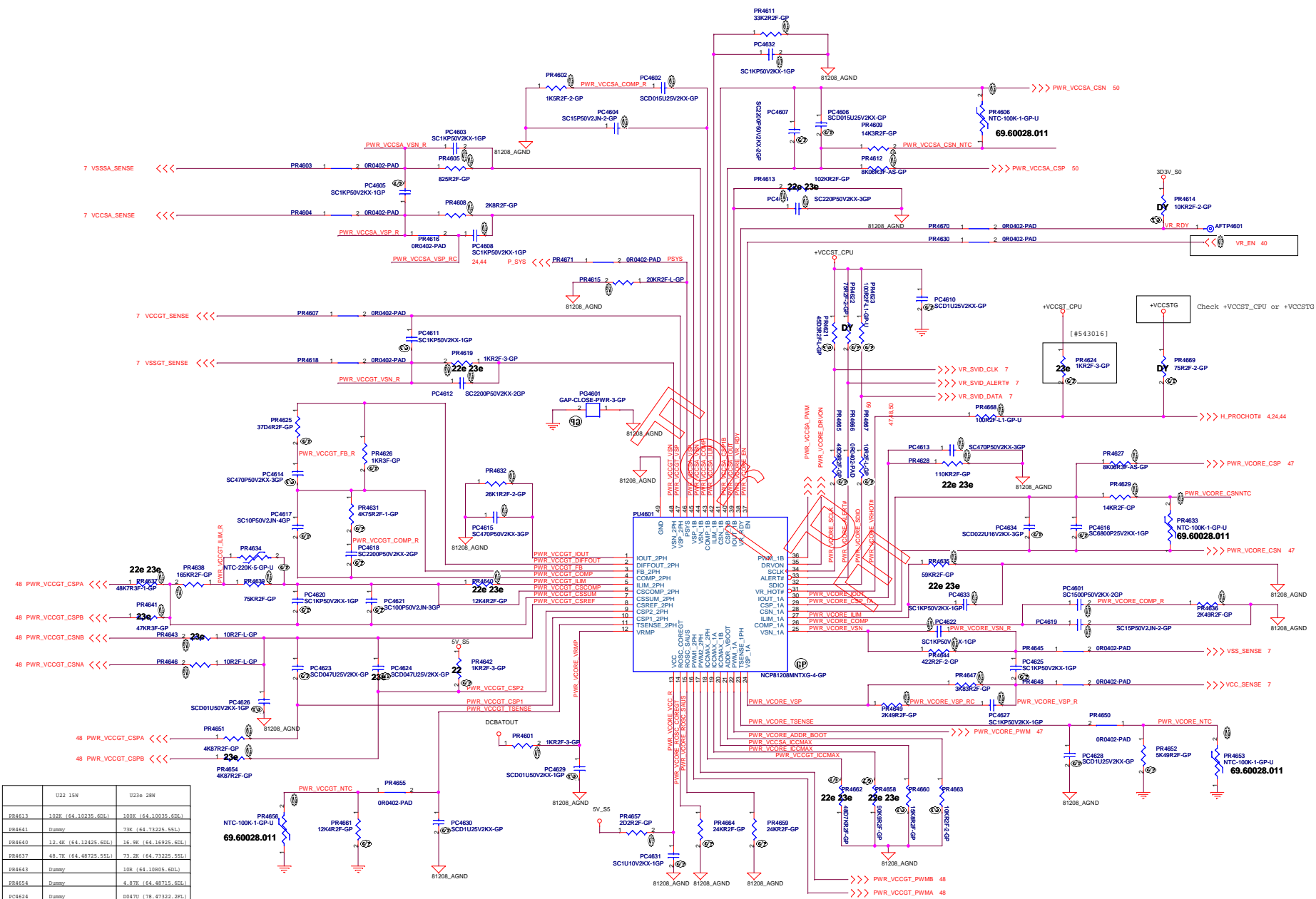
<Core Design>

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Title Connected_Standby(2/2)					
Size A4		Document Number Vegas SKL/KBL-U			Rev A00
Date: Thursday, June 16, 2016		Sheet 42		of 105	

WWW.AllSaler.Com

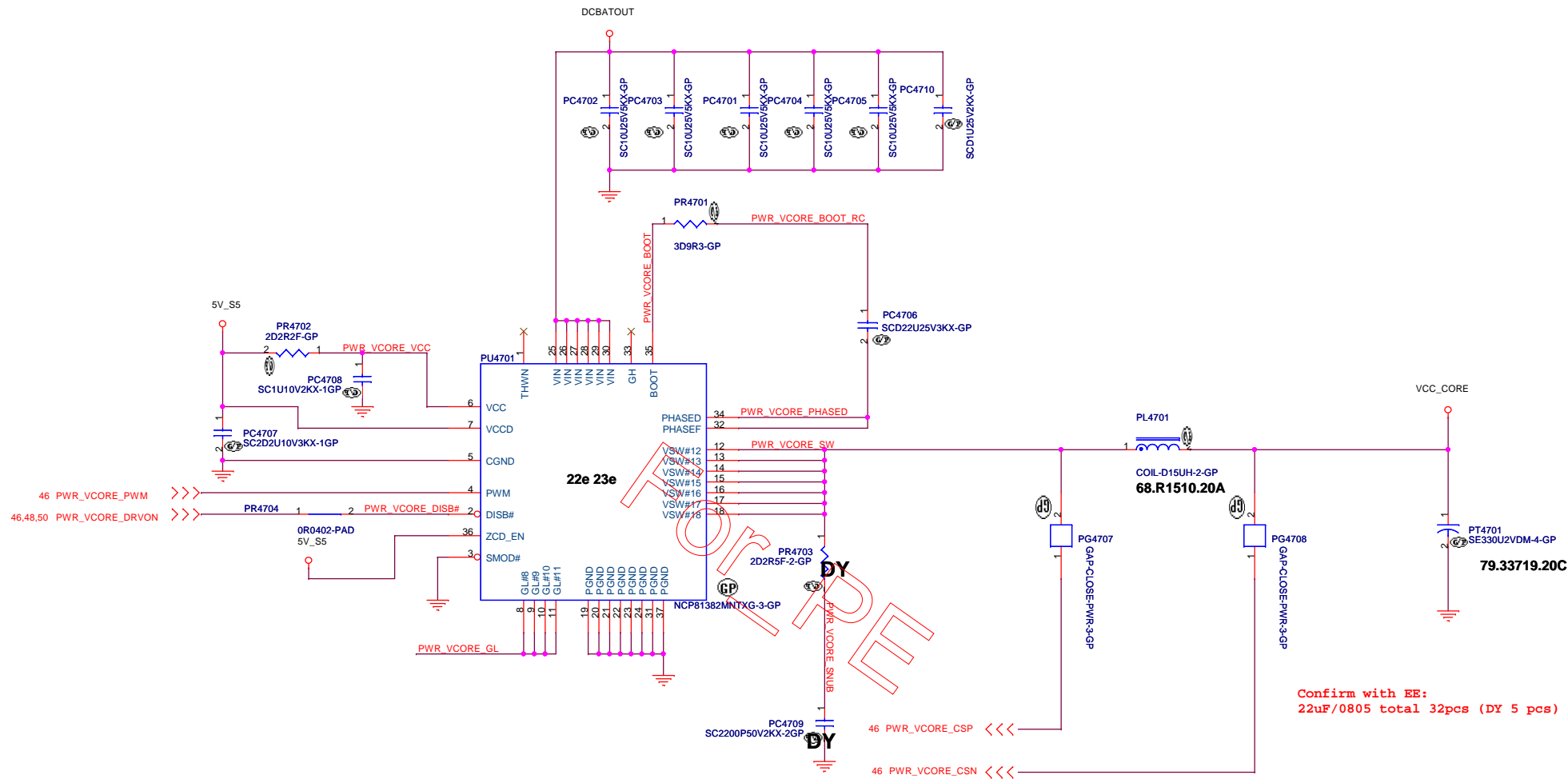






	U22 15W	U236 28W
PR6613	102K (64,10235,62L)	102K (64,10235,62L)
PR6641	Dummy	73K (64,73225,55L)
PR6640	12.4K (64,12425,62L)	26.9K (64,16925,62L)
PR6637	48.7K (64,48725,55L)	73.2K (64,73225,55L)
PR6643	Dummy	108K (64,10805,62L)
PR6654	Dummy	4.87K (64,48715,62L)
PC6624	Dummy	D0470 (78,47322,2P)
PR6642	1K (64,10015,62L)	Dummy
PR6662	48.7K (64,48725,62L)	100K (64,10035,62L)

Main Func = CPU_CORE



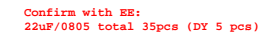
<Core Design>

DELL Wistron Corporation
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Title
NCP81382MN_CPU_VCORE(2/3)

Size A3 Document Number **Vegas SKL/KBL-U** Rev **A00**


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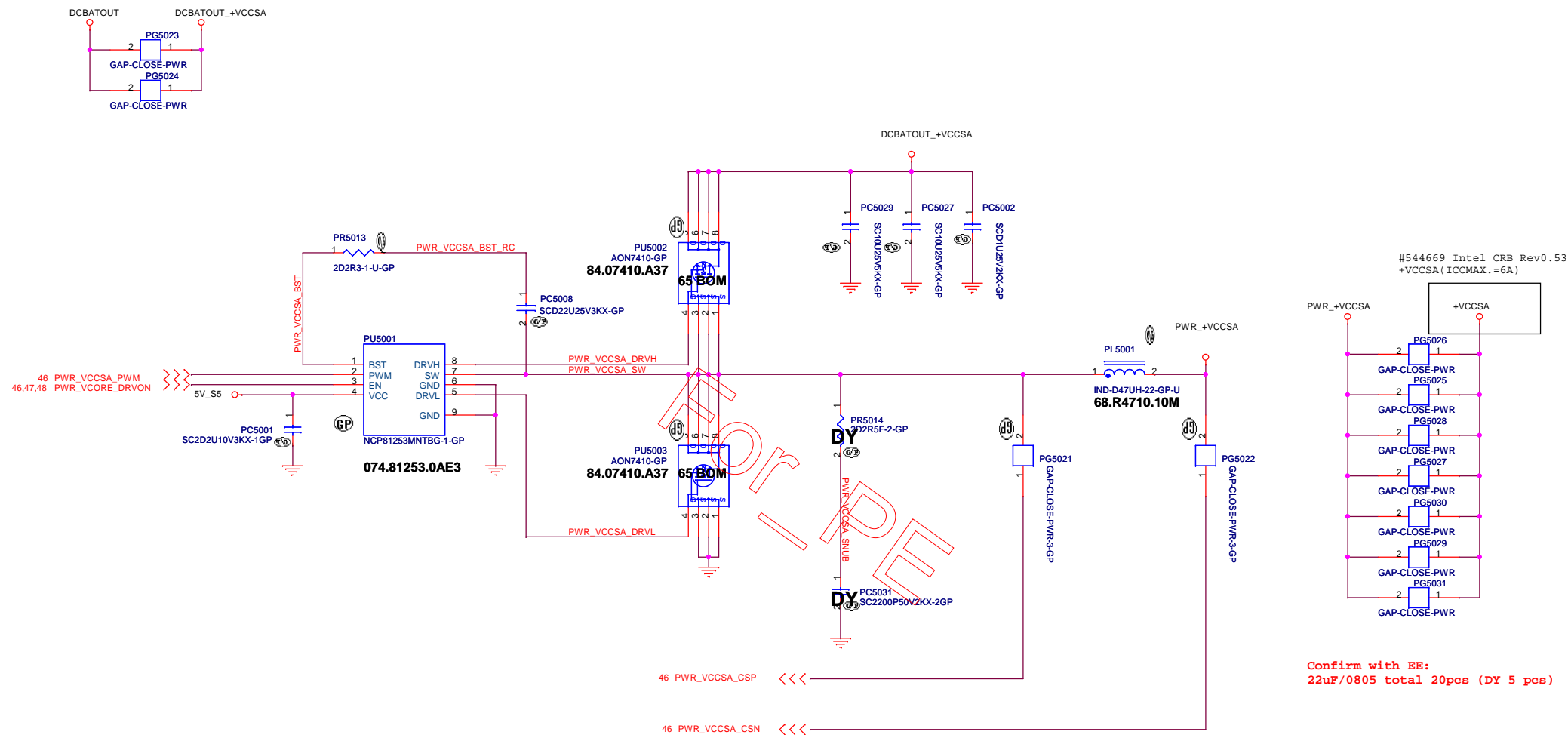
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For PE

<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title NCP81210MN_CPU_VCCGTUS					
Size A4		Document Number Vegas SKL/KBL-U			Rev A00
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Main Func = CPU_CORE

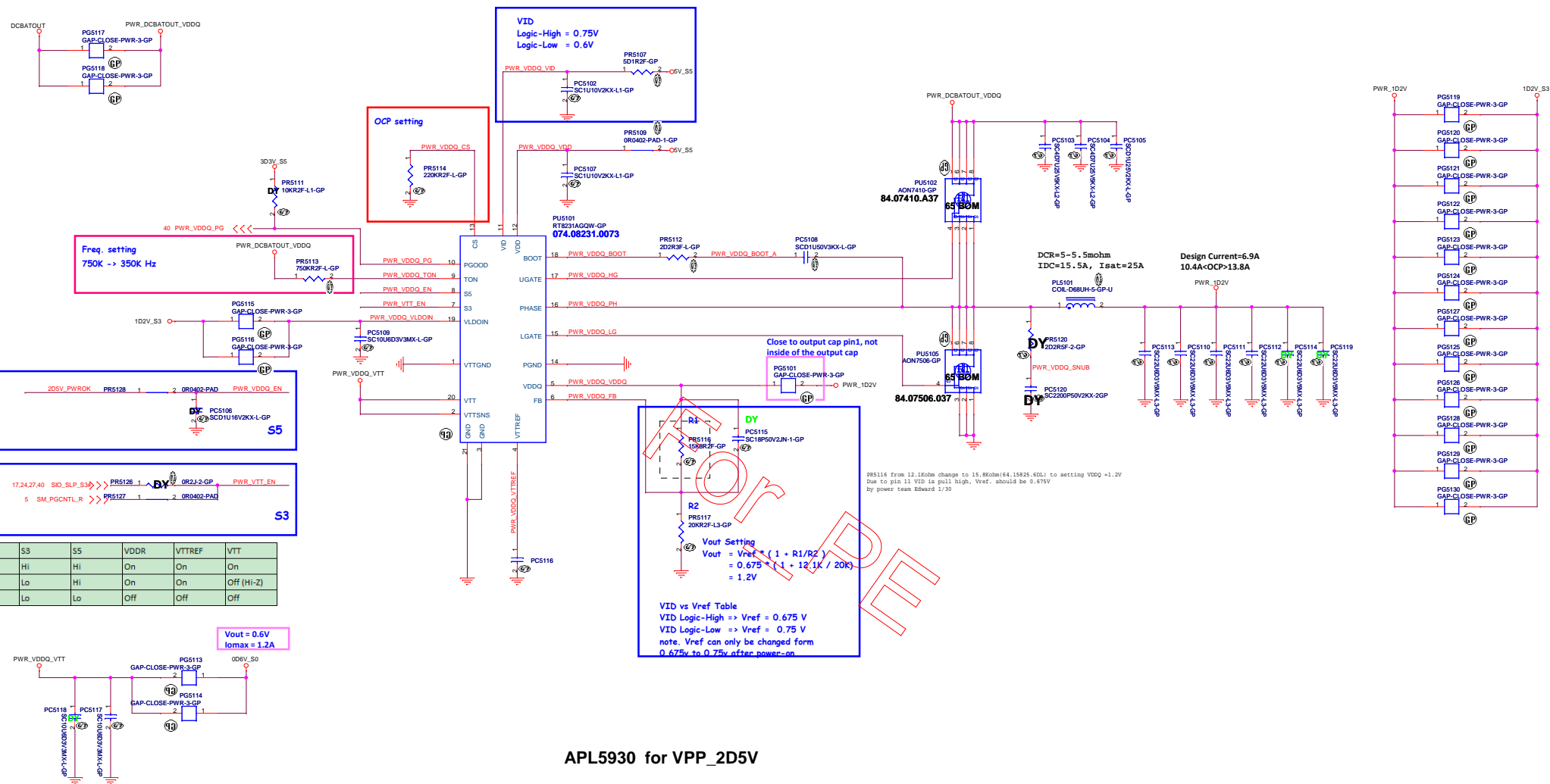
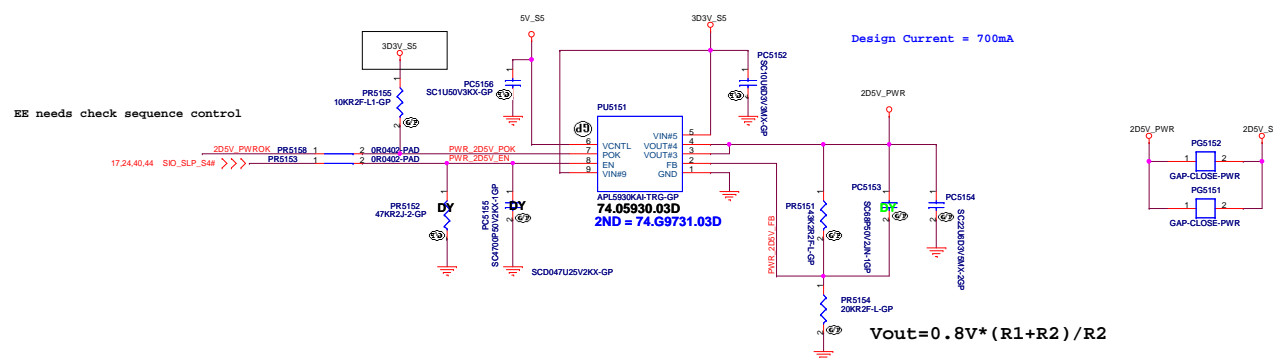


Confirm with EE:
22uF/0805 total 20pcs (DY 5 pcs)

<Core Design>

DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title NCP81253MN_CPU_VCCSA		
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 50 of 105	



```
SSID = PWR.Plane.Regulator_1p2v& 2D5V
```

**APL5930 for VPP_2D5V**

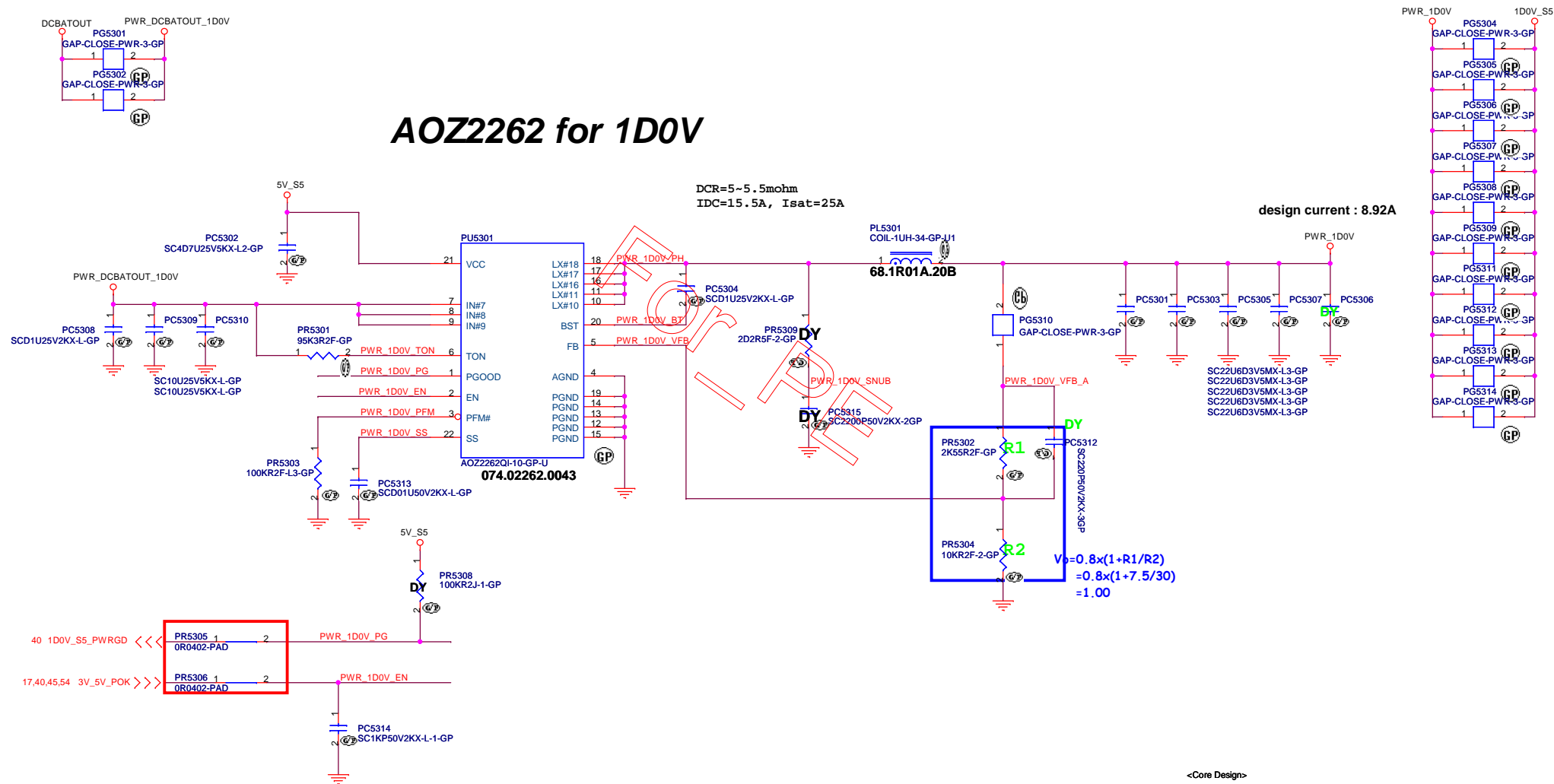
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FOR PFE

<Core Design>

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Title					
(Reserved)					
Size	Document Number				Rev
A4	Vegas SKL/KBL-U				A00
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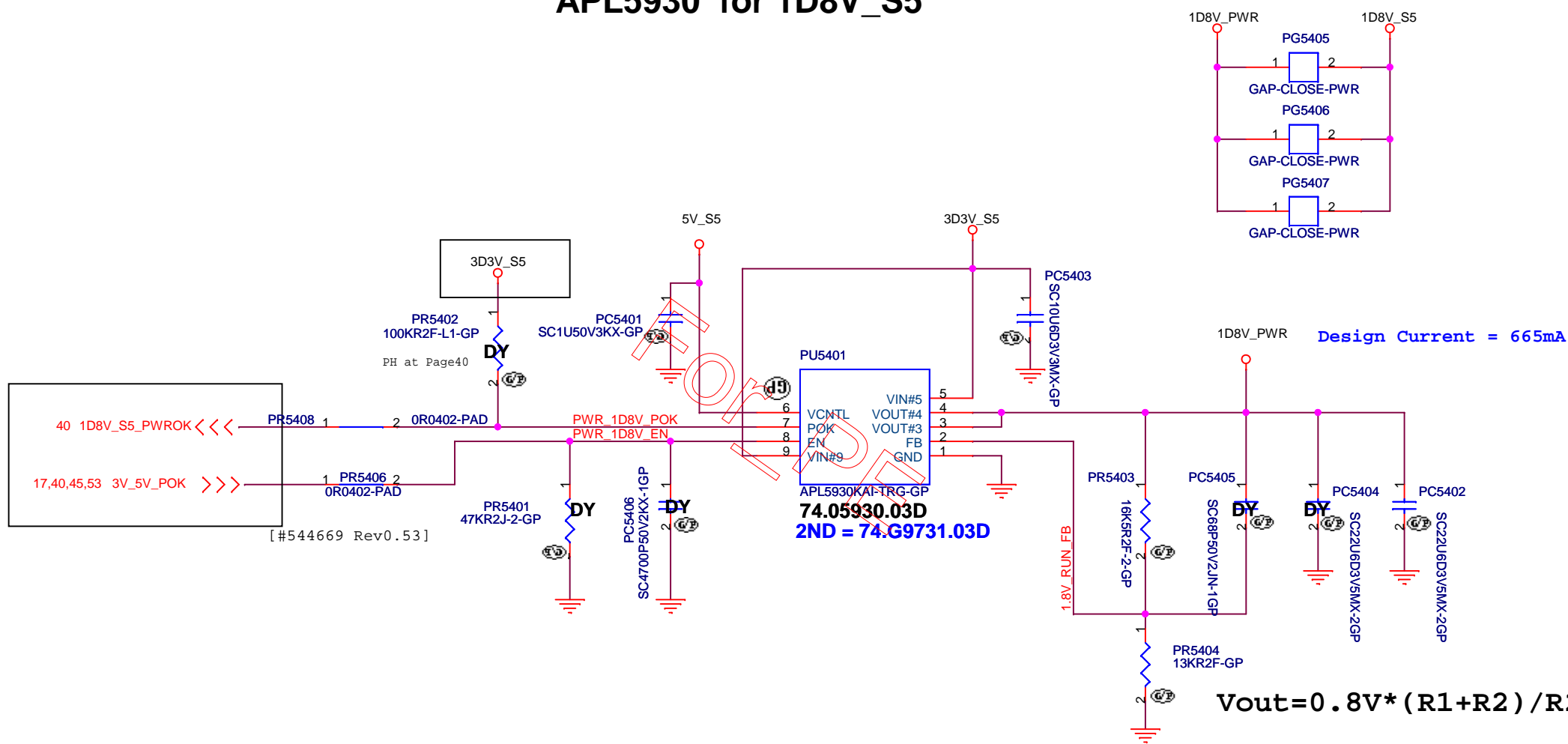
SSID = PWR.Plane.Regulator_1p0v




<Core Design>

Main Func = 1D8V

APL5930 for 1D8V_S5



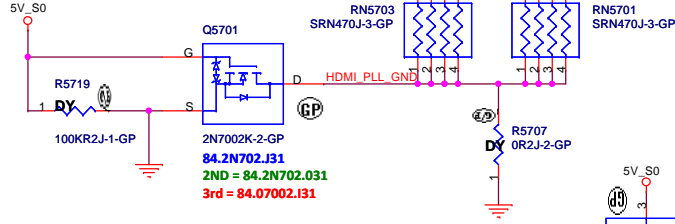
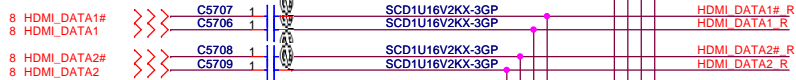
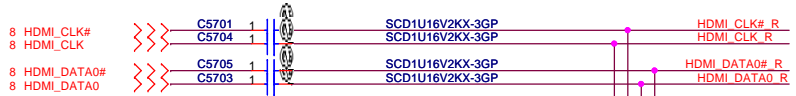
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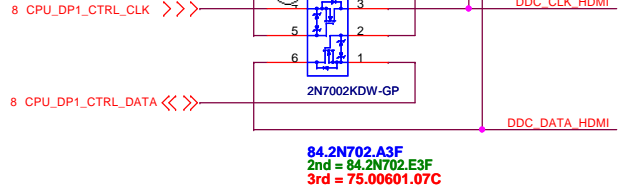
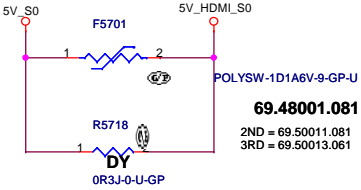
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title LDO-V1D5V&V1D8V		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 54	of 105

Main Func = HDMI

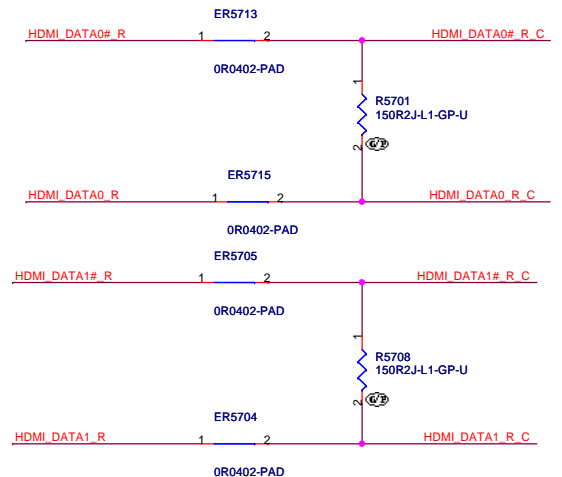
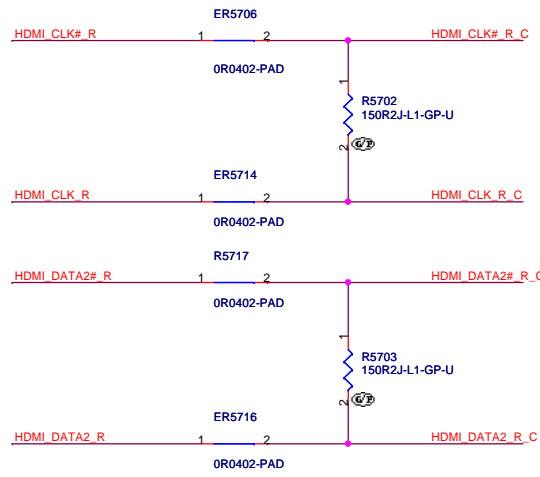
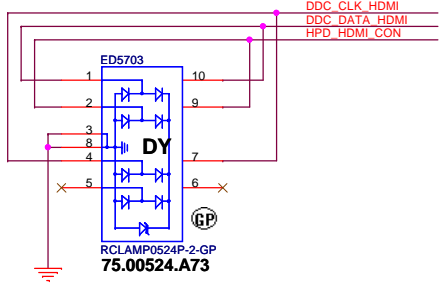
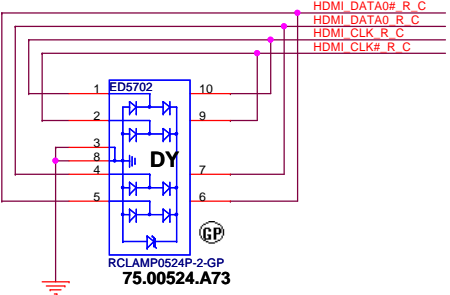
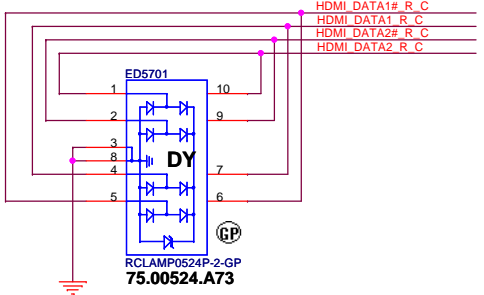


69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend

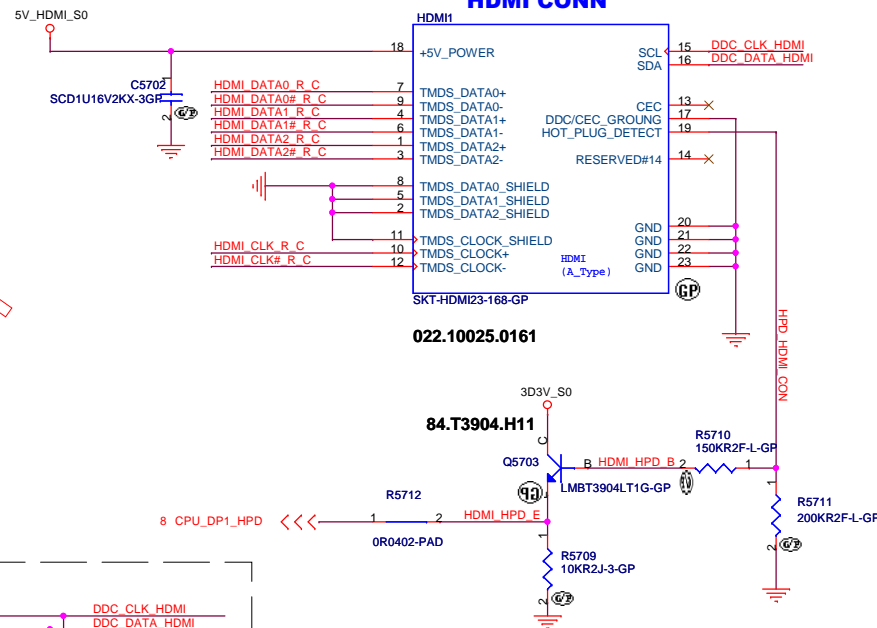


84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

EMI Request:



HDMI CONN



<Core Design>

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Title **HDMI**

Size A3	Document Number Vegas SKL/KBL-U	Rev A00
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For PE

<Core Design>



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Title
(Reserved)

Size
A3

Document Number
Vegas SKL/KBL-U

Rev
A00

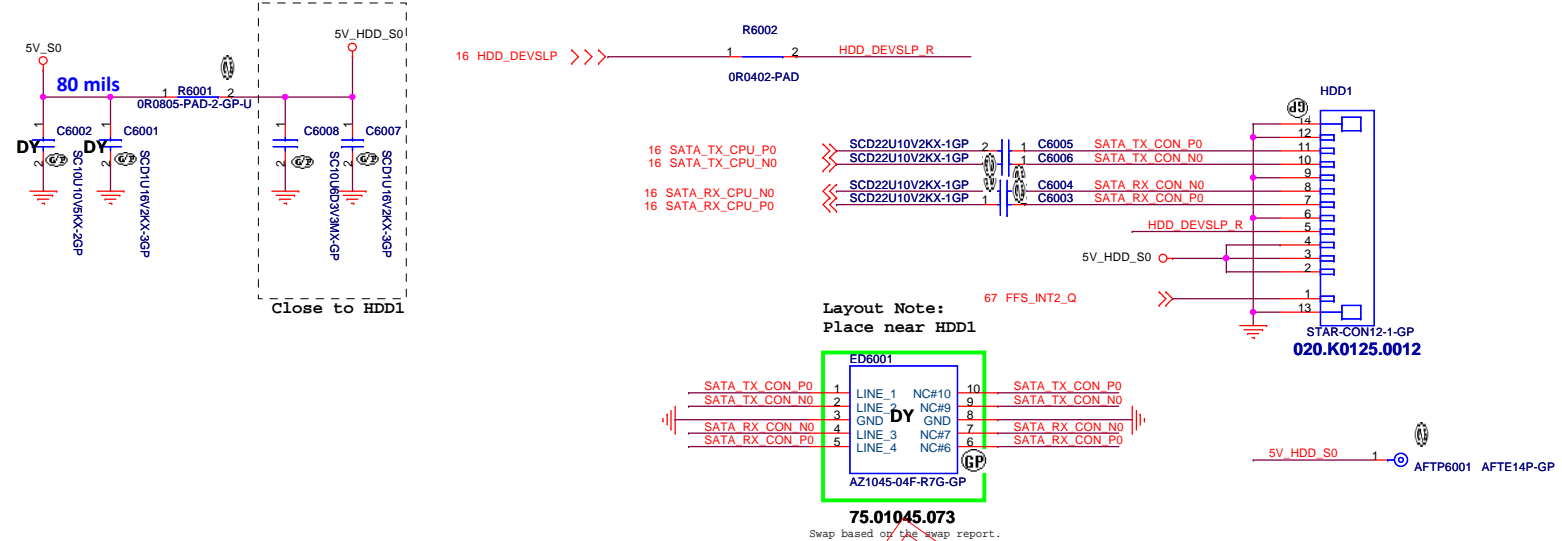
Date: Thursday, June 16, 2016Sheet 58 of 105

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For PE

Main Func = HDD

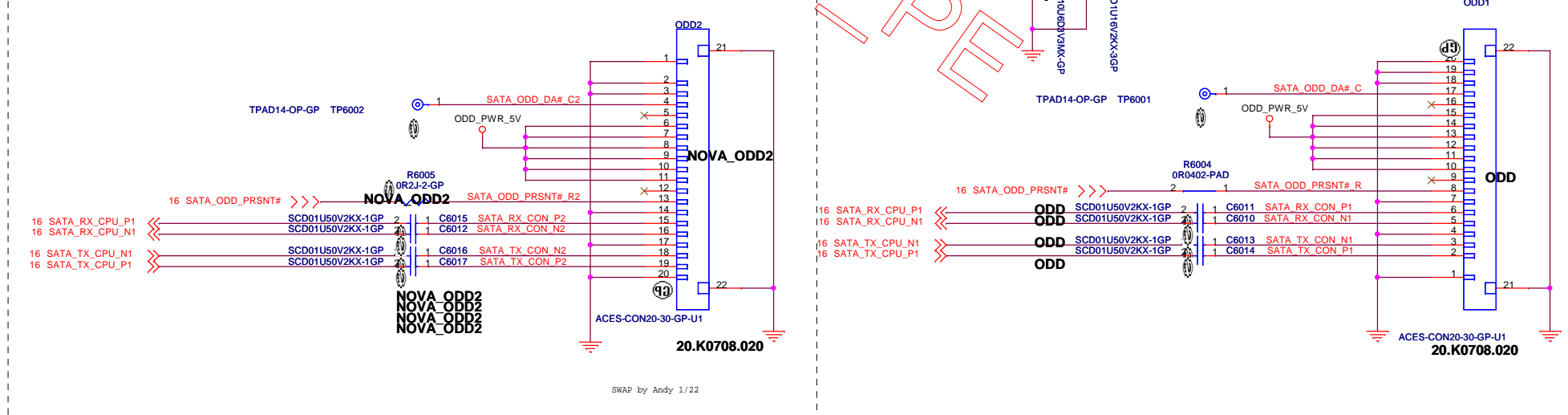
SATA HDD Connector



Main Func = ODD

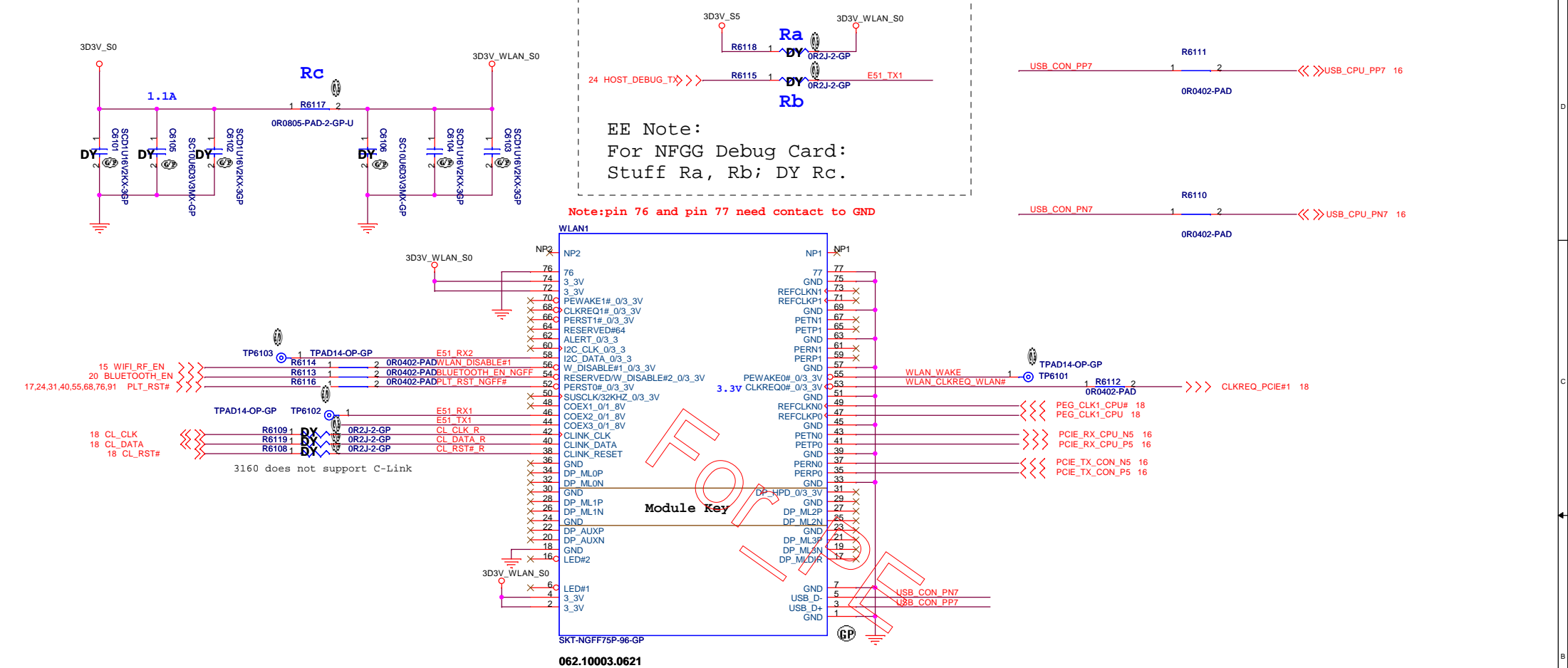
ODD Connector

For NOVA if use ODD2, the cable need to add ont type

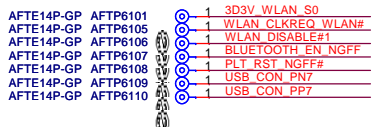


Main Func = WLAN

Reserved for NGFF Debug Card




Support: Intel Dual Band Wireless-AC 3160



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For PE


<Core Design>

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Title					
Reserved					
Size	Document Number				Rev
A4	Vegas SKL/KBL-U				A00
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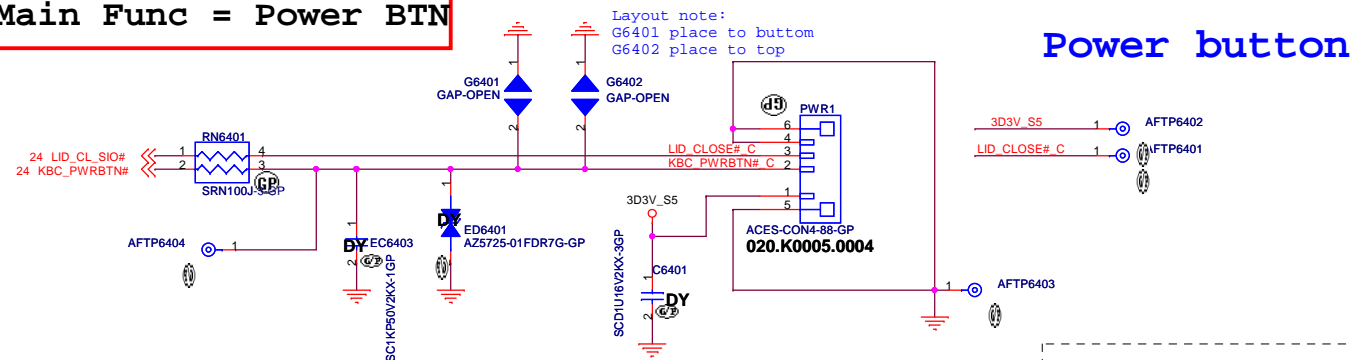
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For PE

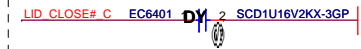
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
Size A4	Document Number Vegas SKL/KBL-U				Rev A00
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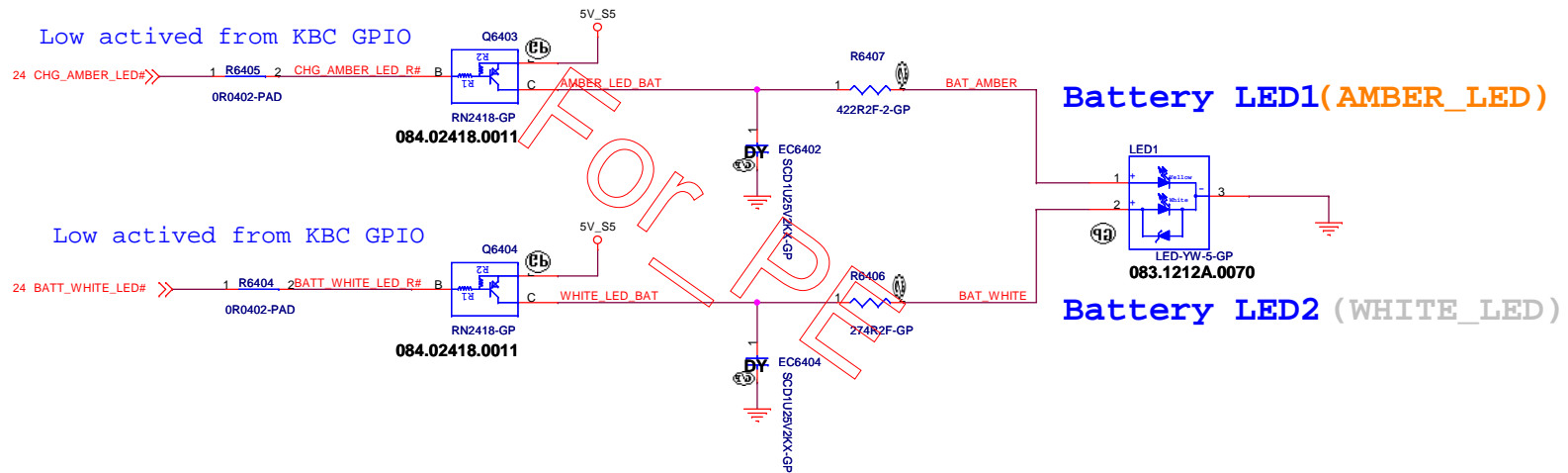
Main Func = Power BTN



For EMI Reserved

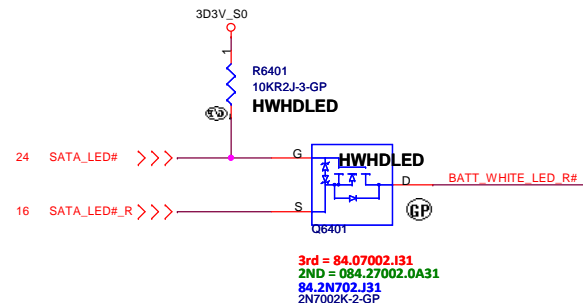


Main Func = Battery LED



Main Func = HDD LED

SATA HDD LED
LOW active from PCH GPIO



<Core Design>



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File			LED Board&Power Button	
Size	Document Number	Rev		
A3	Vegas SKL/KBL-U	A00		
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Main Func = TPAD

Precision Touch Pad Connector

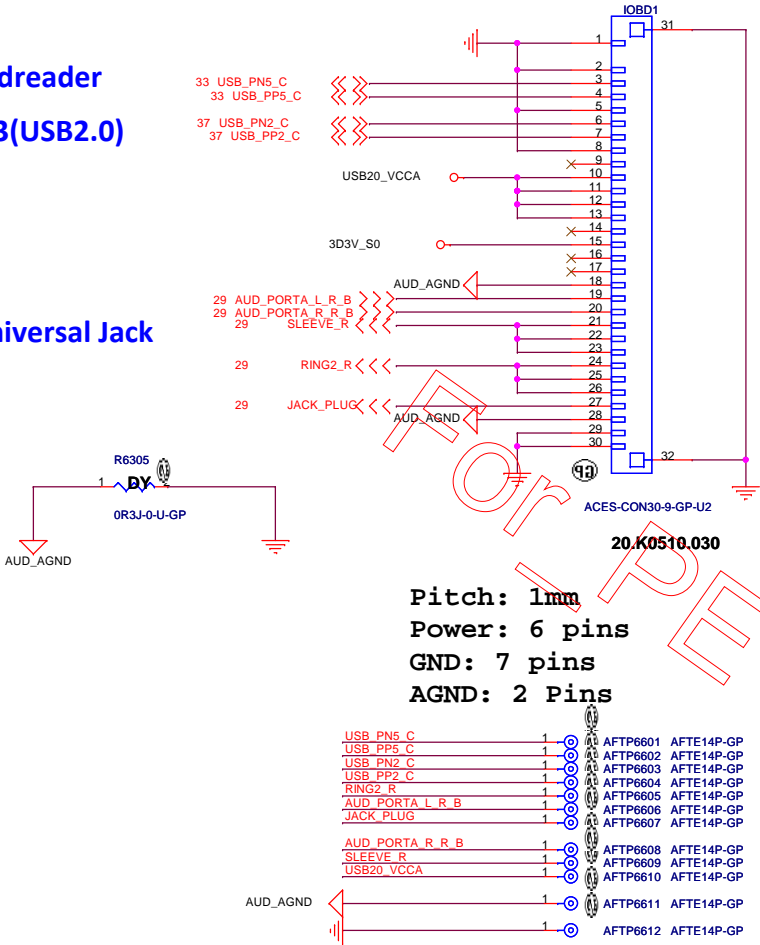


Main Func = IO Connector

I/O Board Connector

Cardreader
USB3(USB2.0)

Universal Jack



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins

USB_PN5_C	1	AFTP6601	AFTE14P-GP
USB_PP5_C	1	AFTP6602	AFTE14P-GP
USB_PN2_C	1	AFTP6603	AFTE14P-GP
USB_PP2_C	1	AFTP6604	AFTE14P-GP
RING2_R	1	AFTP6605	AFTE14P-GP
AUD_PORTA_L_R_B	1	AFTP6606	AFTE14P-GP
JACK_PLUG	1	AFTP6607	AFTE14P-GP
AUD_PORTA_R_R_B	1	AFTP6608	AFTE14P-GP
SLEEVE_R	1	AFTP6609	AFTE14P-GP
USB2_VCCA	1	AFTP6610	AFTE14P-GP
AUD_AGND	1	AFTP6611	AFTE14P-GP
	1	AFTP6612	AFTE14P-GP

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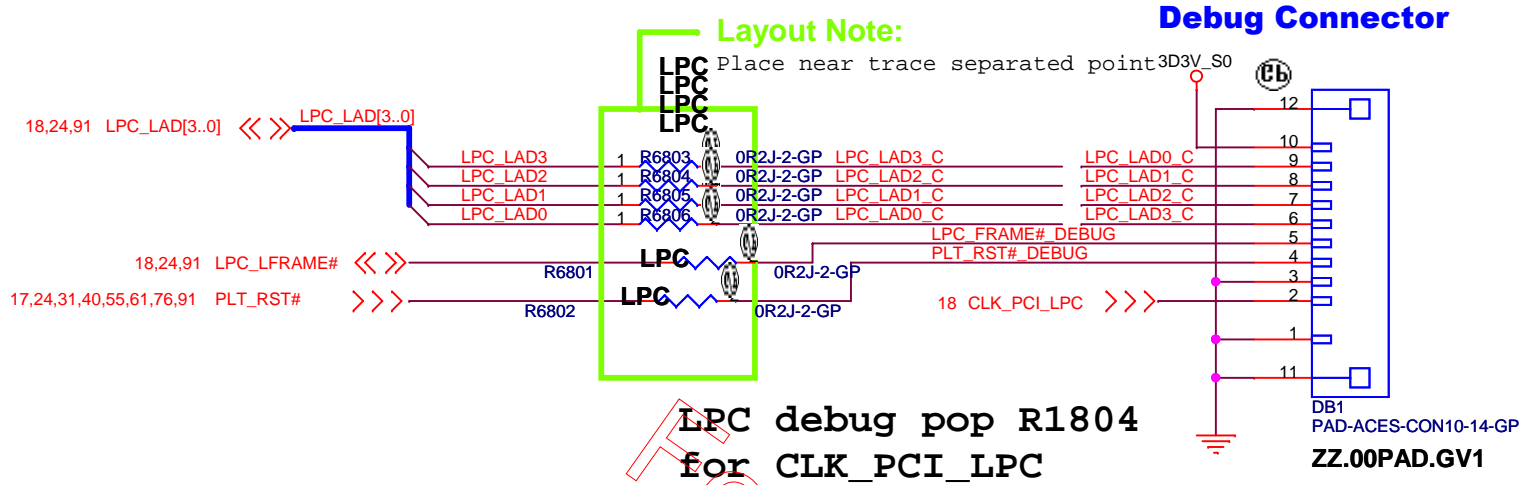
<Core Design>



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Title			IO Board Connector		
Size			Document Number		
A3			Vegas SKL/KBL-U		
Date: Monday, June 27, 2016			Sheet 66 of 105		
			Rev A00		

Main Func = Debug



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.


<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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For PE


<Core Design>

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Reserved			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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FOR PE


<Core Design>

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Title (Reserved)			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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FOR PE

<Core Design>

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RESERVED		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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For PE

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB3.0 PORT			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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FOR PE

<Core Design>

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Title Reserved			
Size A4	Document Number Vegas SKL/KBL-U		Rev A00
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For PE

<Core Design>

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Title			
Reserved			
Size A3	Document Number Vegas SKL/KBL-U		Rev A00
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For PE

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Vegas SKL/KBL-U		Rev A00
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Main Func = dGPU

Table 3-5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3 V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100 MHz (± 300 ppm) input frequency; 0 V to 0.7 V single ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.68-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω
GPU1A

1 OF 7

16 PEG_TX_GPU_P0
16 PEG_TX_GPU_N0

16 PEG_TX_GPU_P1
16 PEG_TX_GPU_N1

16 PEG_TX_GPU_P2
16 PEG_TX_GPU_N2

16 PEG_TX_GPU_P3
16 PEG_TX_GPU_N3

>>>
>>>
>>>
>>>

AF30
AC31

AE29
AD28

AD30
AC31

AC29
AB28

PCIE_RX0P
PCIE_RX0N

PCIE_RX1P
PCIE_RX1N

PCIE_RX2P
PCIE_RX2N

PCIE_RX3P
PCIE_RX3N

AB30
AA31

PCIE_RX4P
PCIE_RX4N

AA29
Y28

PCIE_RX5P
PCIE_RX5N

Y30
W31

PCIE_RX6P
PCIE_RX6N

W29
V28

PCIE_RX7P
PCIE_RX7N

Y30
U31

NC#V30
NC#U31

U29
T28

NC#U29
NC#T28

T30
R31

NC#T30
NC#R31

R29
P28

NC#R29
NC#P28

P30
N31

NC#P30
NC#N31

N29
M28

NC#N29
NC#M28

M30
L31

NC#M30
NC#L31

L29
K30

NC#L29
NC#K30

PCIE_TX0P
PCIE_TX0N

PCIE_TX1P
PCIE_TX1N

PCIE_TX2P
PCIE_TX2N

PCIE_TX3P
PCIE_TX3N

PCIE_TX4P
PCIE_TX4N

PCIE_TX5P
PCIE_TX5N

PCIE_TX6P
PCIE_TX6N

PCIE_TX7P
PCIE_TX7N

NC#W24
NC#W23

NC#V27
NC#U26

NC#U24
NC#U23

NC#T26
NC#T27

NC#T24
NC#T23

NC#P27
NC#P26

NC#P24
NC#P23

NC#M27
NC#N26

GEN2/GEN3
GEN2/GEN3
GEN2/GEN3
GEN2/GEN3

SCD1U16V2KX-3GP
SCD1U16V2KX-3GP
SCD1U16V2KX-3GP
SCD1U16V2KX-3GP

PEG_RX_CPU_P0 16
PEG_RX_CPU_N0 16
PEG_RX_CPU_P1 16
PEG_RX_CPU_N1 16
PEG_RX_CPU_P2 16
PEG_RX_CPU_N2 16
PEG_RX_CPU_P3 16
PEG_RX_CPU_N3 16

PCI EXPRESS INTERFACE

CLOCK
PCIE_REFCLKP
PCIE_REFCLKN

TEST_PG
PERST#

JET-XT-S3-GP

OPS

CALIBRATION

PCIE_CALR_TX

PCIE_CALR_RX

Y22

AA22

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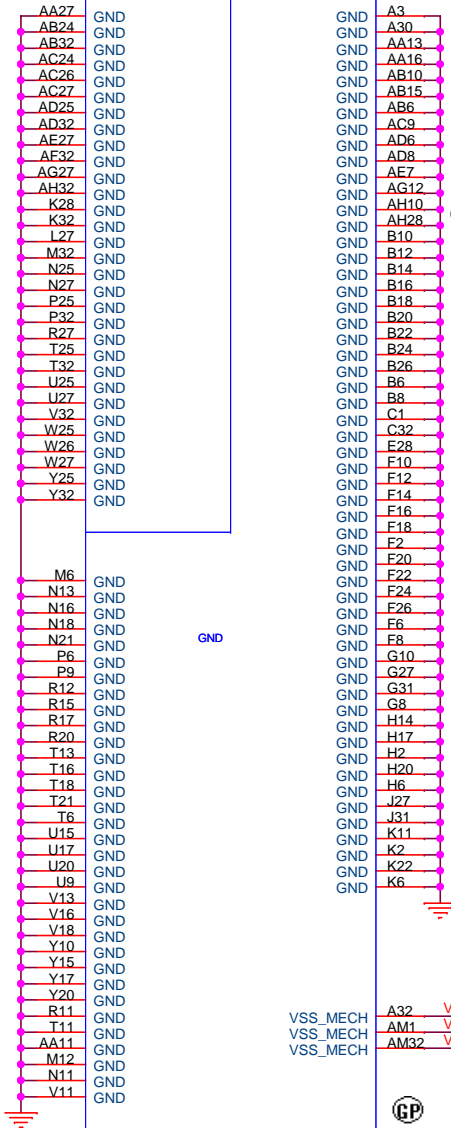
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Main Func = dGPU

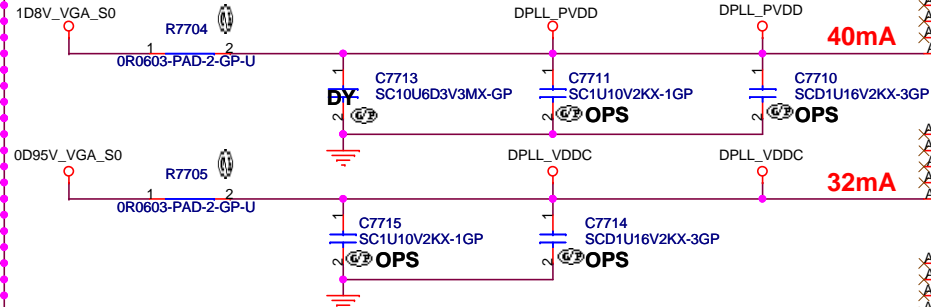
GPU1E

5 OF 7



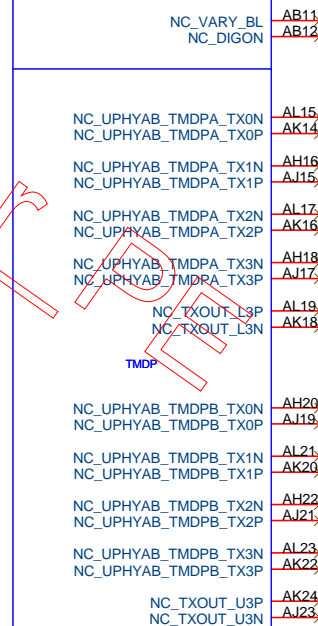
OPS

1.8V and 0.95V for Clock resource



GPU1F

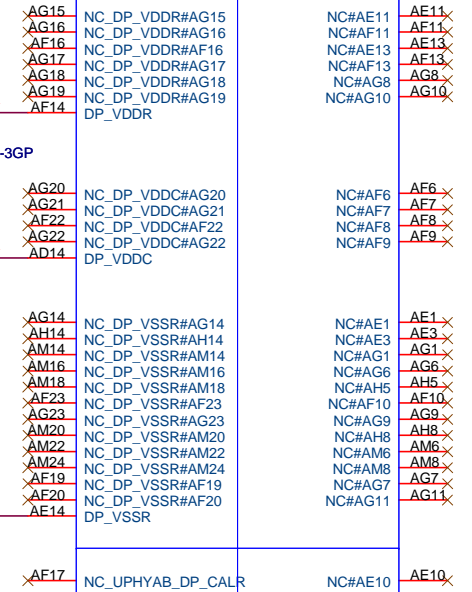
6 OF 7



OPS

GPU1G

7 OF 7



JET-XT-S3-GP

OPS

<Core Design>

緯創資通

Wistron Corporation

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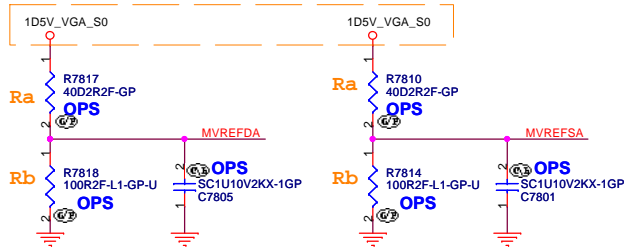
Title			
077_GPU (2/5) DIGITALOUT			
Size	Project Name		Rev
	Vegas SKL/KBL-U		X00
Date:	Friday, June 24, 2016	Sheet	77 of 105

Main Func = dGPU

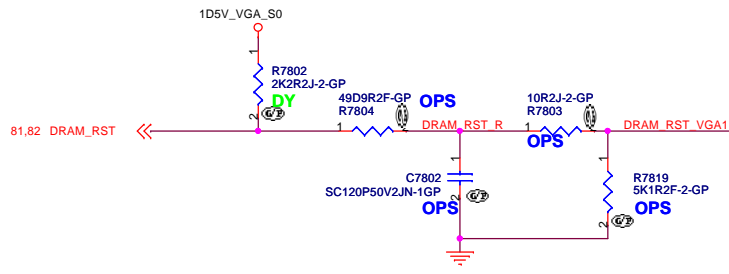
Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

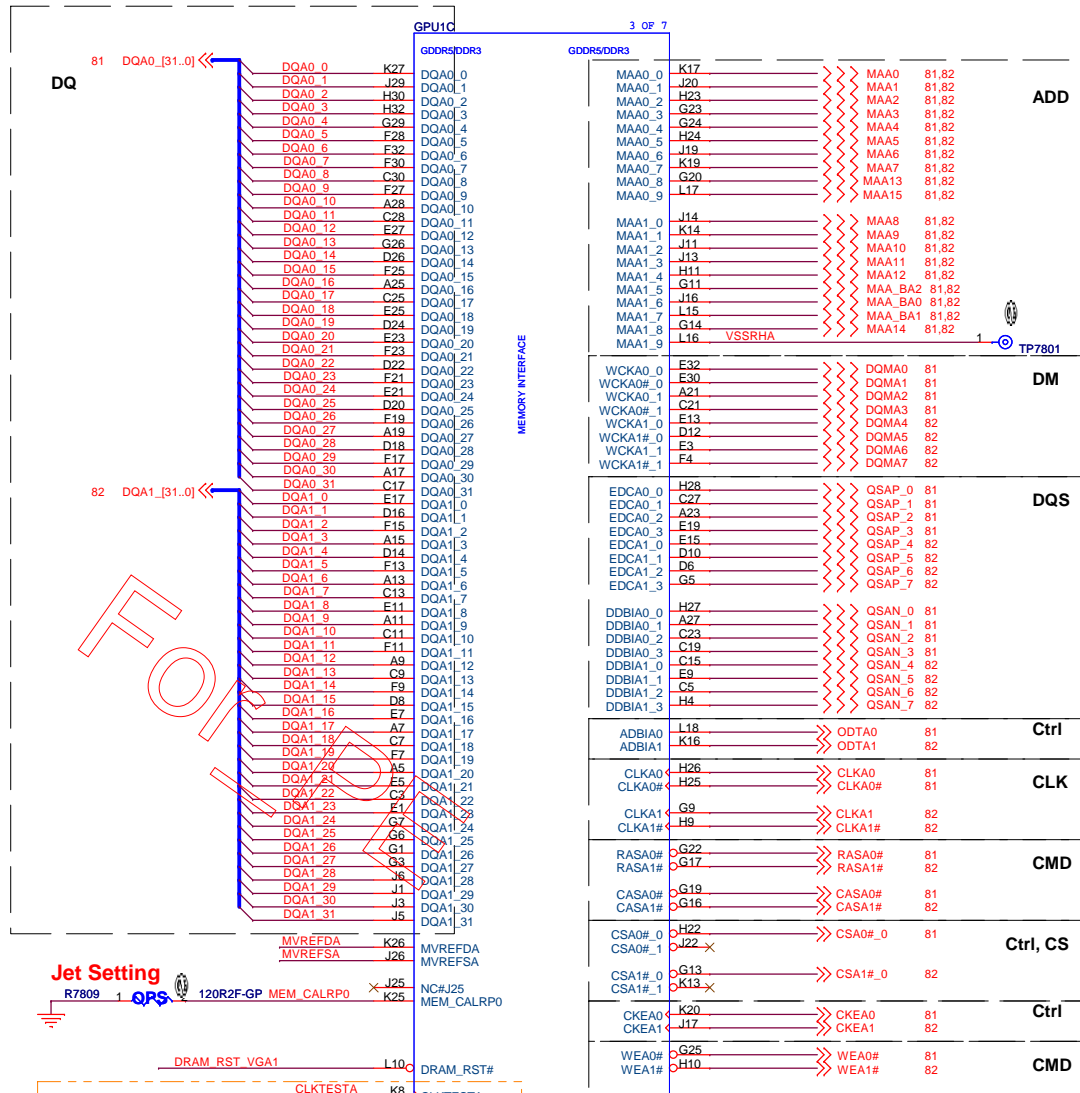
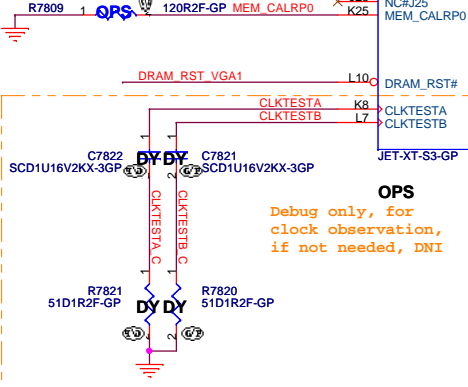
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR3



Jet Setting



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Title	078_GPU (3/5) VRAM I/F	Rev
Size	Project Name	Vegas SKL/KBL-U
Date	Monday, June 27, 2016	Sheet 78 of 105

A horizontal line with a point labeled '5' on it.

A horizontal line with a tick mark on the left and a label 'd' on the right.

1

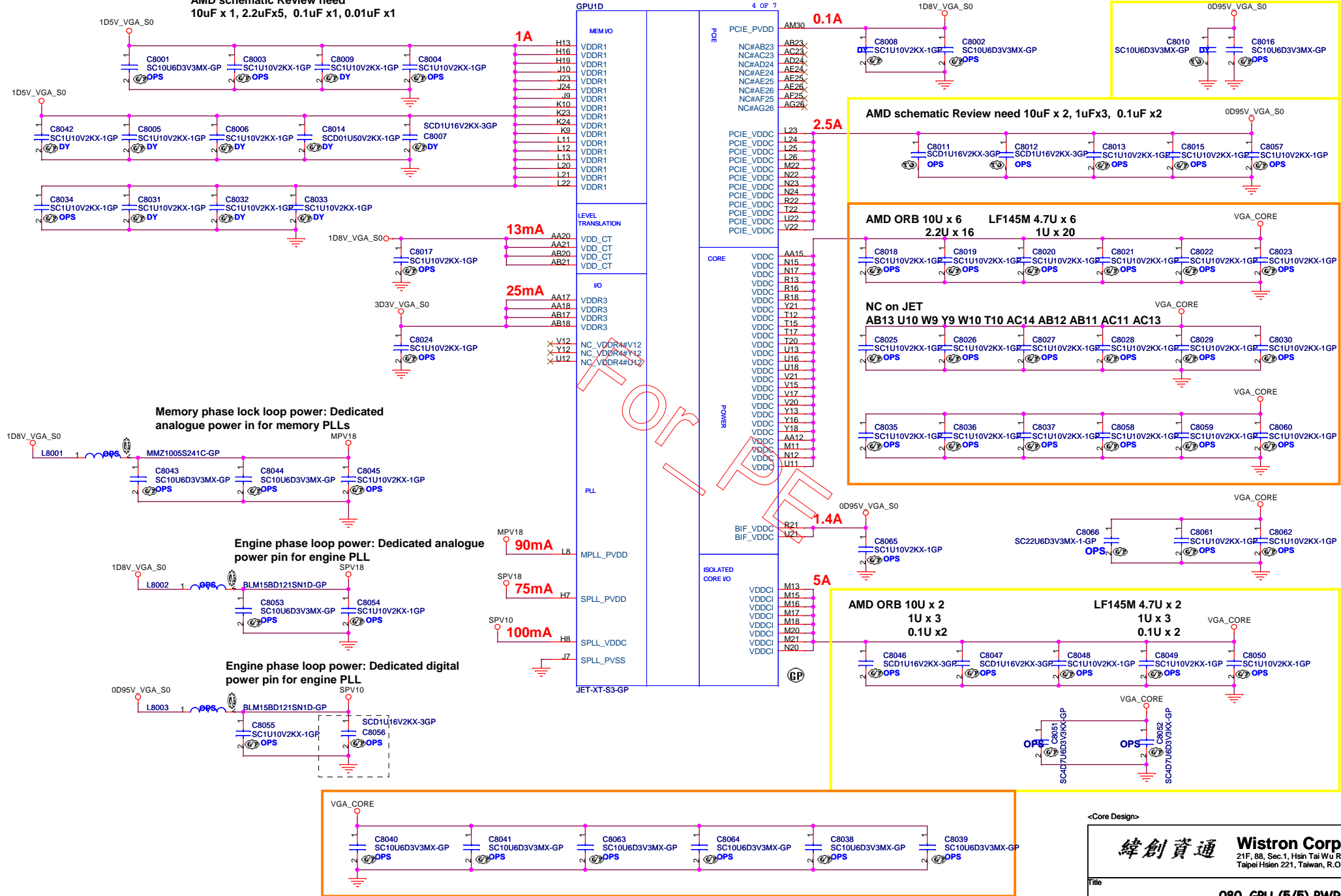
3

Title		079_GPU (4/5) G
Size	Project Name	
	Vegas SKL/	
Date	Monday, June 27, 2016	Revised

TRAP	
	Nav
of	Not

Main Func = dGPU

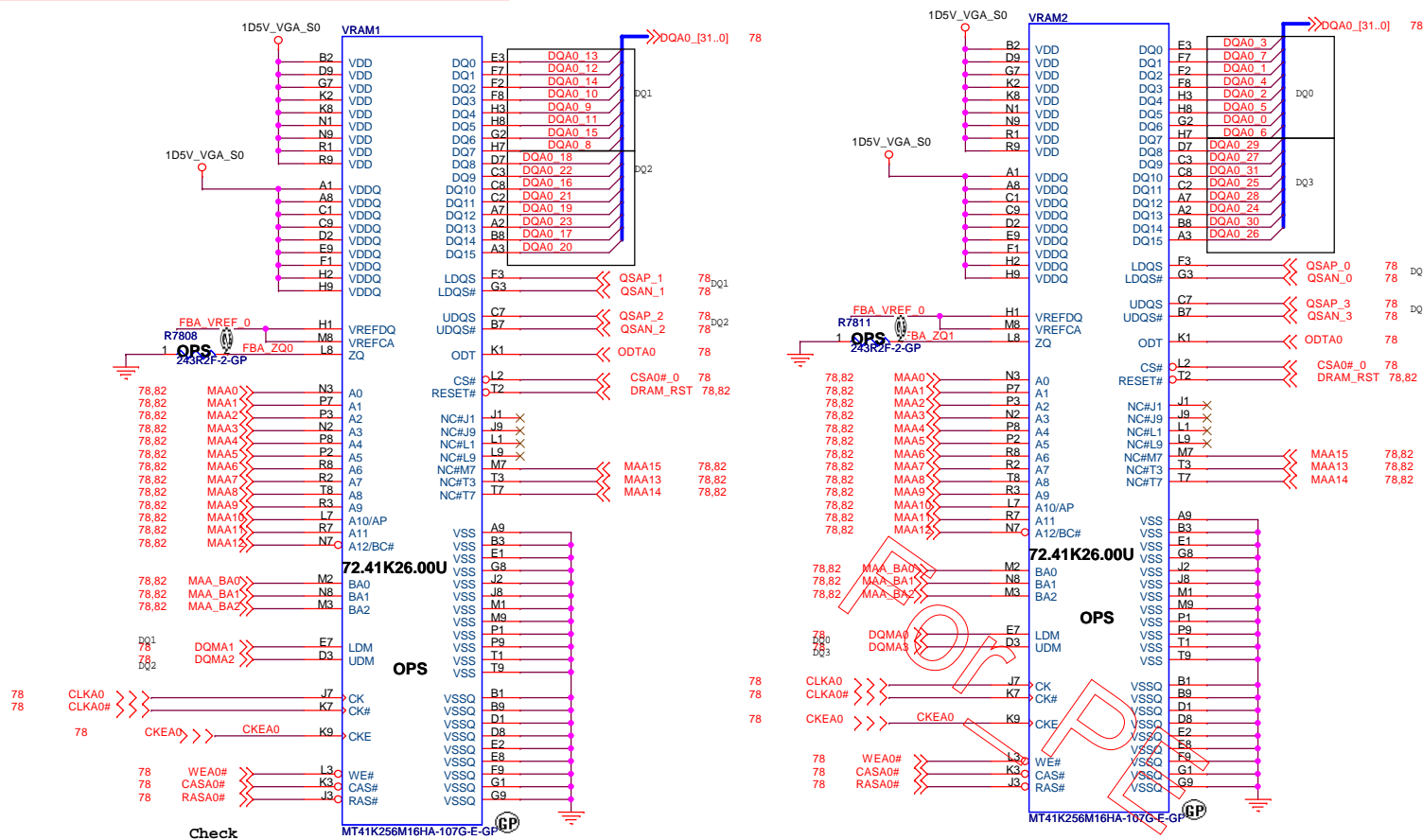
AMD schematic Review need
10uF x 1, 2.2uF x5, 0.1uF x1, 0.01uF x1



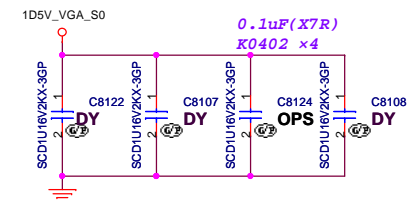
<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	080_GPU (5/5) PWR/GND	
Size	Project Name	Rev
<Project Name>		
Date: Thursday, June 16, 2016	Sheet 80	of 105

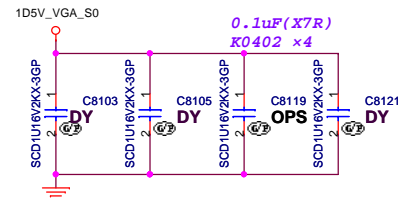
Main Func = Vram (DDR3L)



Place close VRAM1VDDQ ball

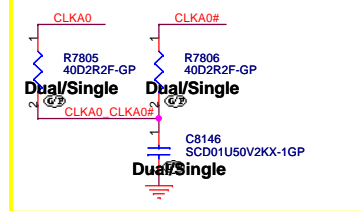


Place close VRAM2 VDD ball

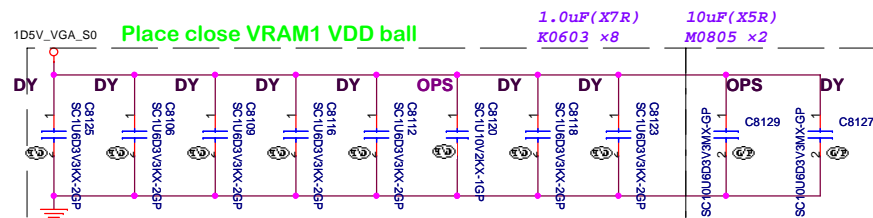
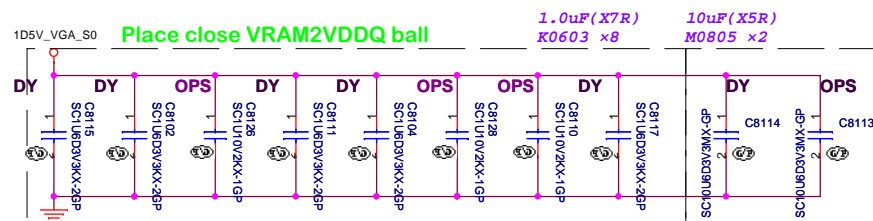
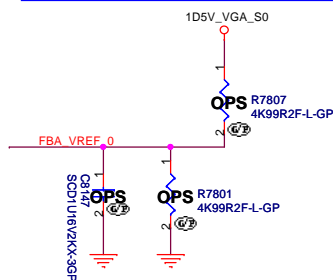


R7805 R7810

Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL

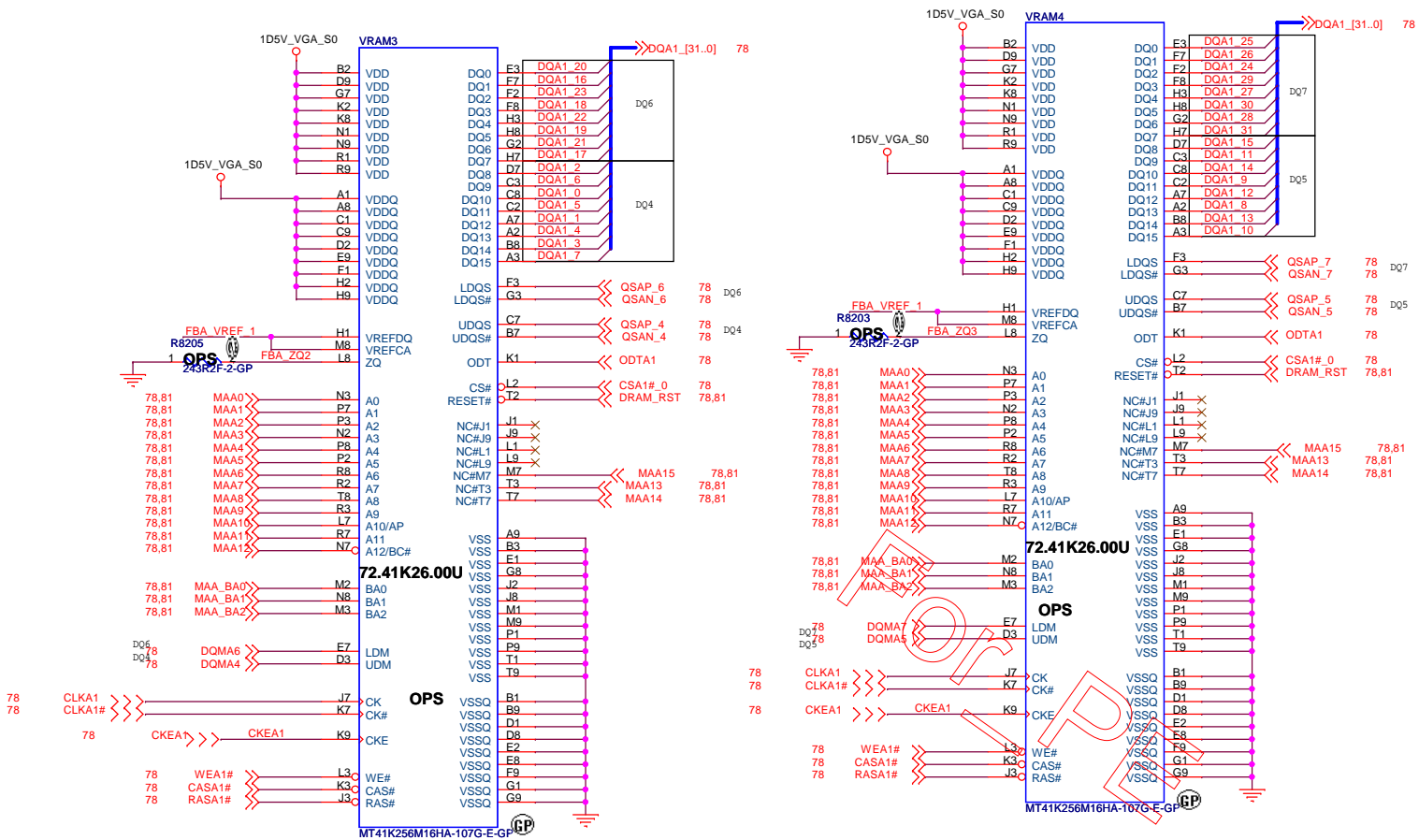


Frame Buffer Partition A-Lower Half



<Core Design>


Main Func = Vram (DDR3L)



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For PE

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Title

GPU-VRAM5,6 (3/4)

Size
A3

Document Number
Vegas SKL/KBL-U

Rev
A00

Date: Thursday, June 16, 2016

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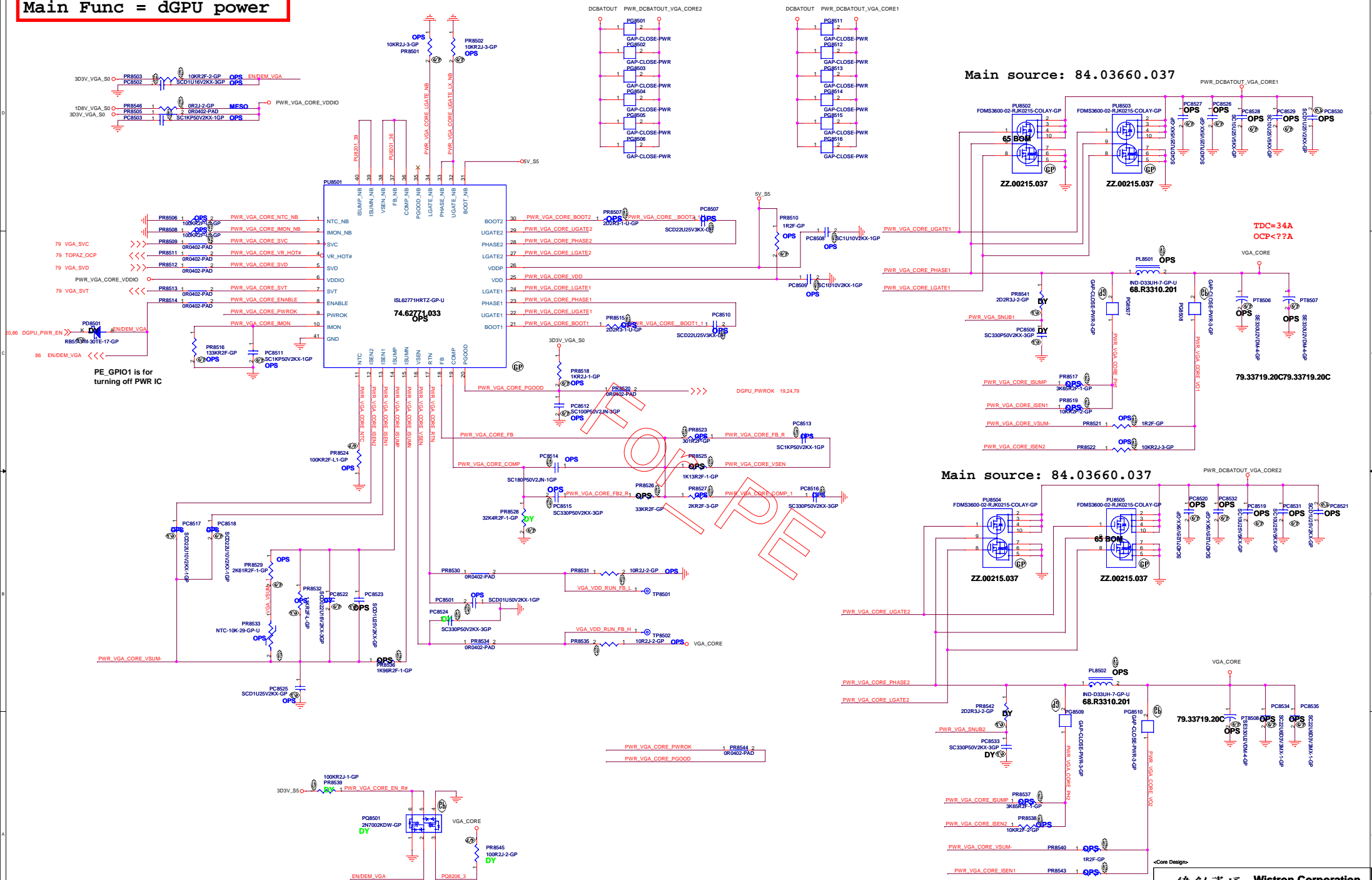
FOR P/E

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<Core Design>

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Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number		Rev
A3	Vegas SKL/KBL-U		A00
Date:	Thursday, June 16, 2016	Sheet	84 of 105

Main Func = dGPU power



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		Wistron Corporation 217, 88, Sec. 1, Hsin Tai Wu Rd., Hsuehli, Taipei Hsien 221, Taiwan, R.O.C.	
GPU Discrete Power			
Vegas SKL/KBL-U		A00	
Date: Monday, June 27, 2016	Email:	of:	105

Close Pin1

$V_o = 0.6 \times (1 + R1/R2)$
 $= 0.6 \times (1 + 30.1/51.1)$
 $= 0.953$

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Title		
Reserved		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016	Sheet 87 of	105

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<Core Design>



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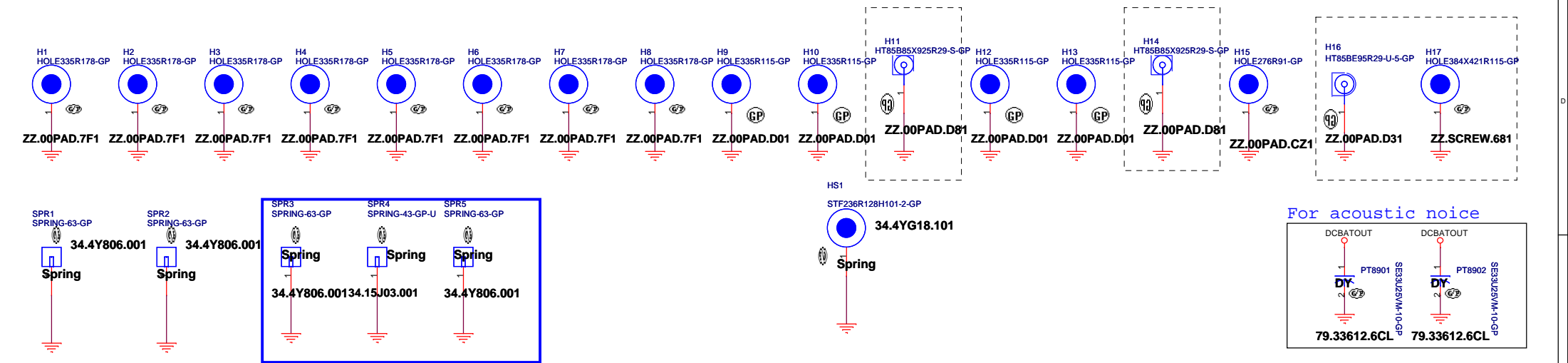
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

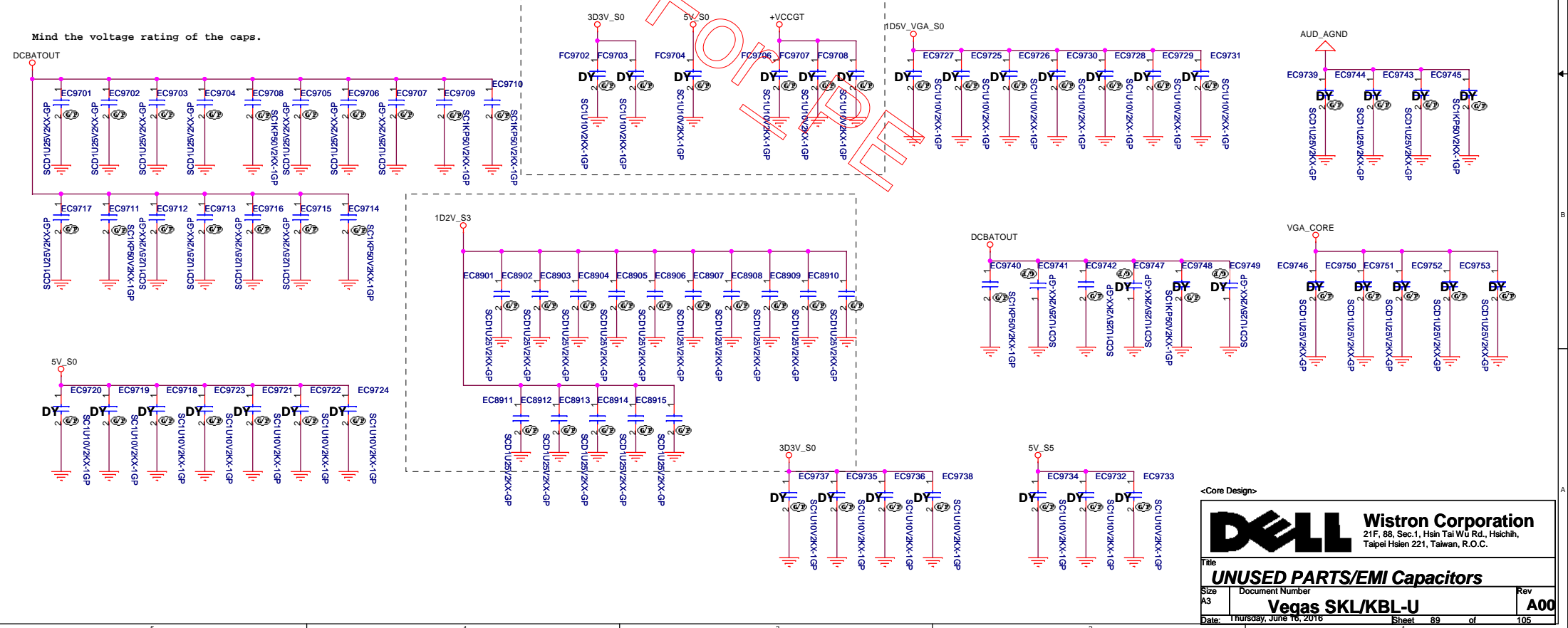
Reserved

Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016	Sheet 88 of	105

Main Func = UnusedParts



Main Func = EMI & RF Capacitors



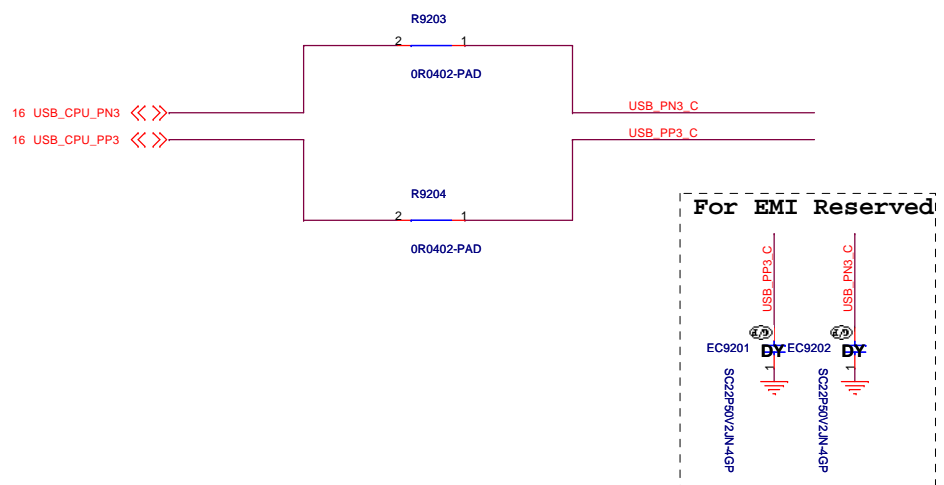
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For PE

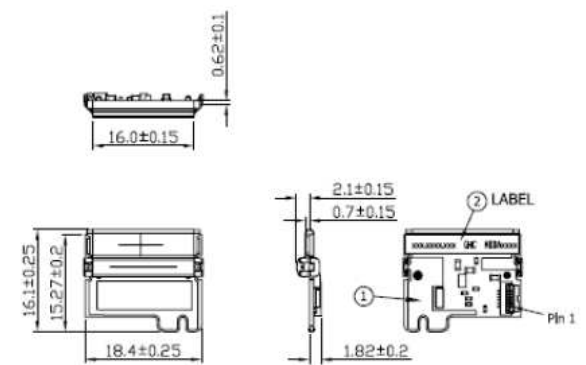
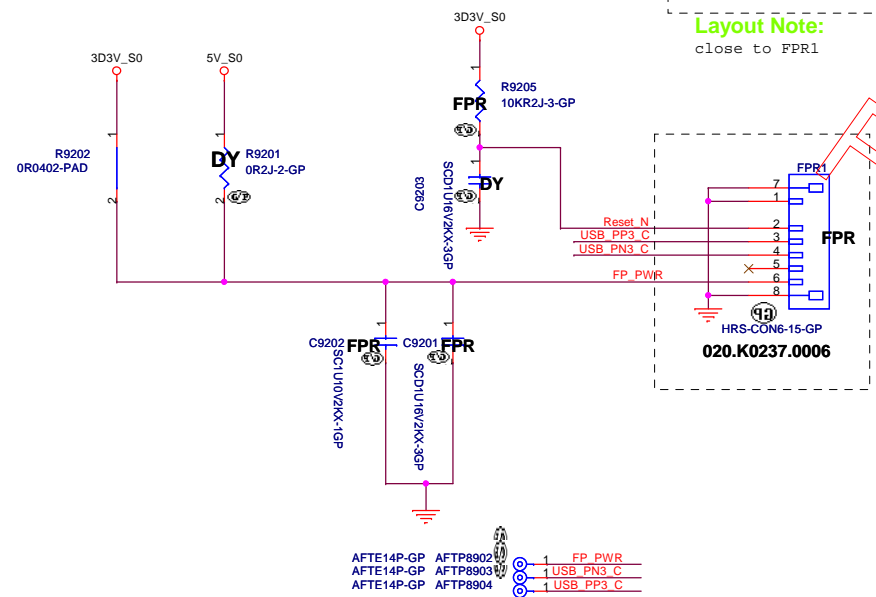
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Title		
Reserved		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
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SSID = Finger Print

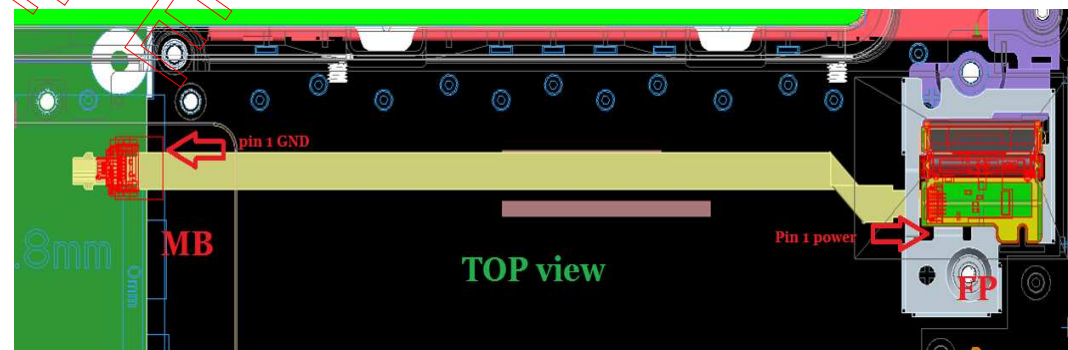


Layout Note:
close to FPR1



Note :
Module:
1.Sensor Type;Semiconductor
2.Interface:USB 1.0 and 2.0 Full Speed

FingerPrint Pin Assignments.
Pin 1 = 3.3VIn
Pin 2 = (ND)
Pin 3 = D-
Pin 4 = D+
Pin 5 = Reset_N
Pin 6 = GND




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(Blanking)

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Title

(Reserved)

Size	Document Number	Rev
A3	Vegas SKL/KBL-U	A00

Date: Thursday, June 16, 2016	Sheet 94 of 105
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Title (Reserved)		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016		Sheet 96 of 105

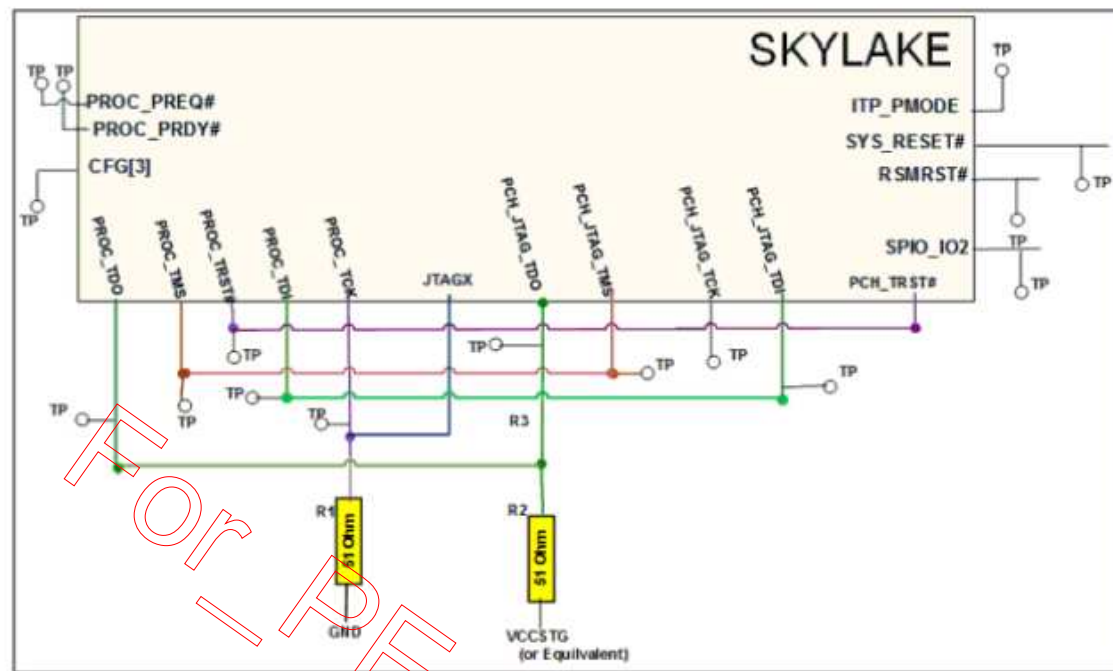
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Title		
LVDS_Switch		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016	Sheet 97 of	105

PCH_JTAG_TMS test point
XDP_TMS test point
PCH_JTAG_TDI test point
XDP_TDI test point
XDP_TCLK test point
XDP_TCK_JTAGX test point
XDP_TDO_CPU test point
PCH_JTAG_TDO test point



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Title

CPU XDP;PCH XDP

Size

Document Number

Rev

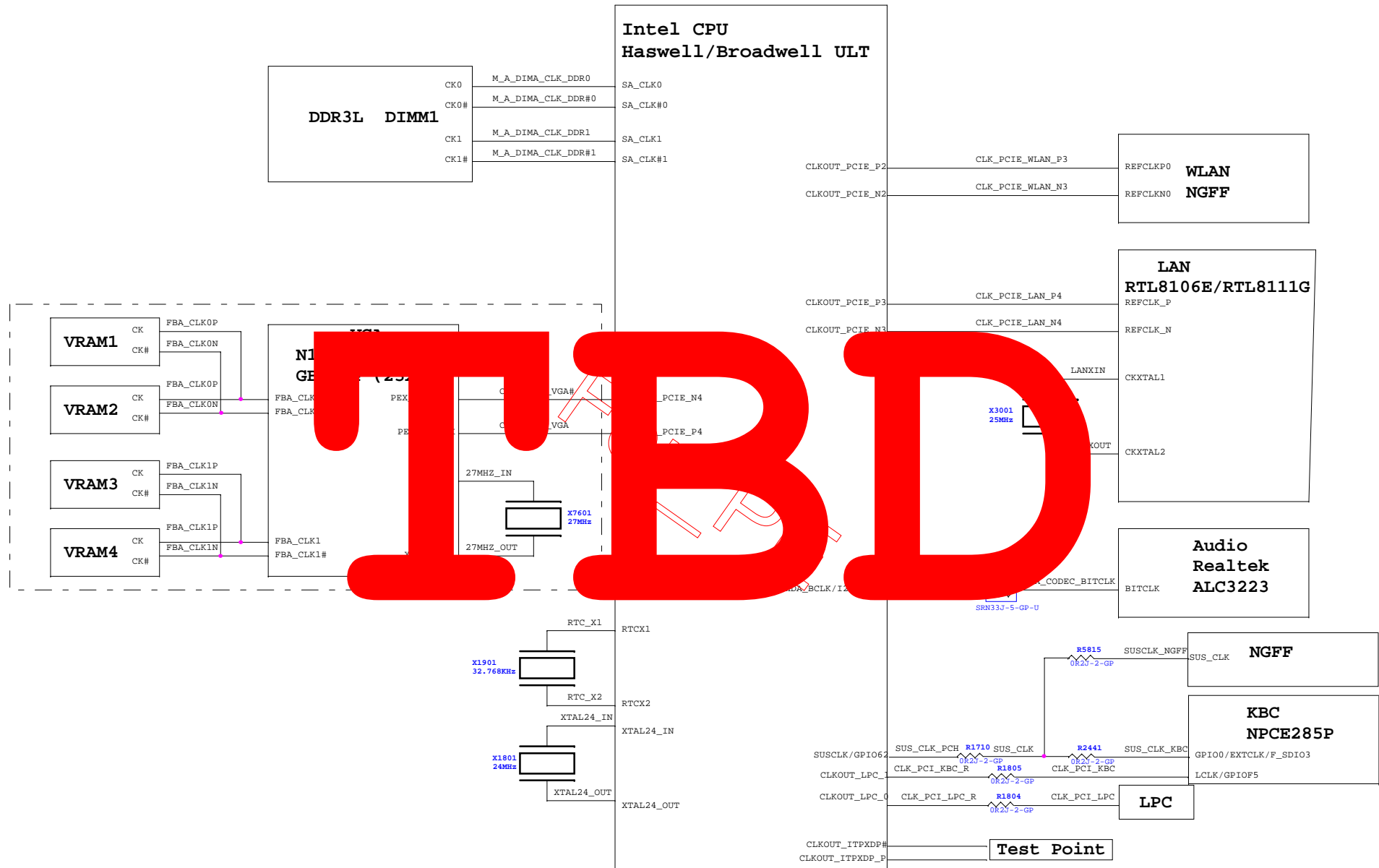
Vegas SKL/KBL-U

A00

Date: Thursday, June 16, 2016

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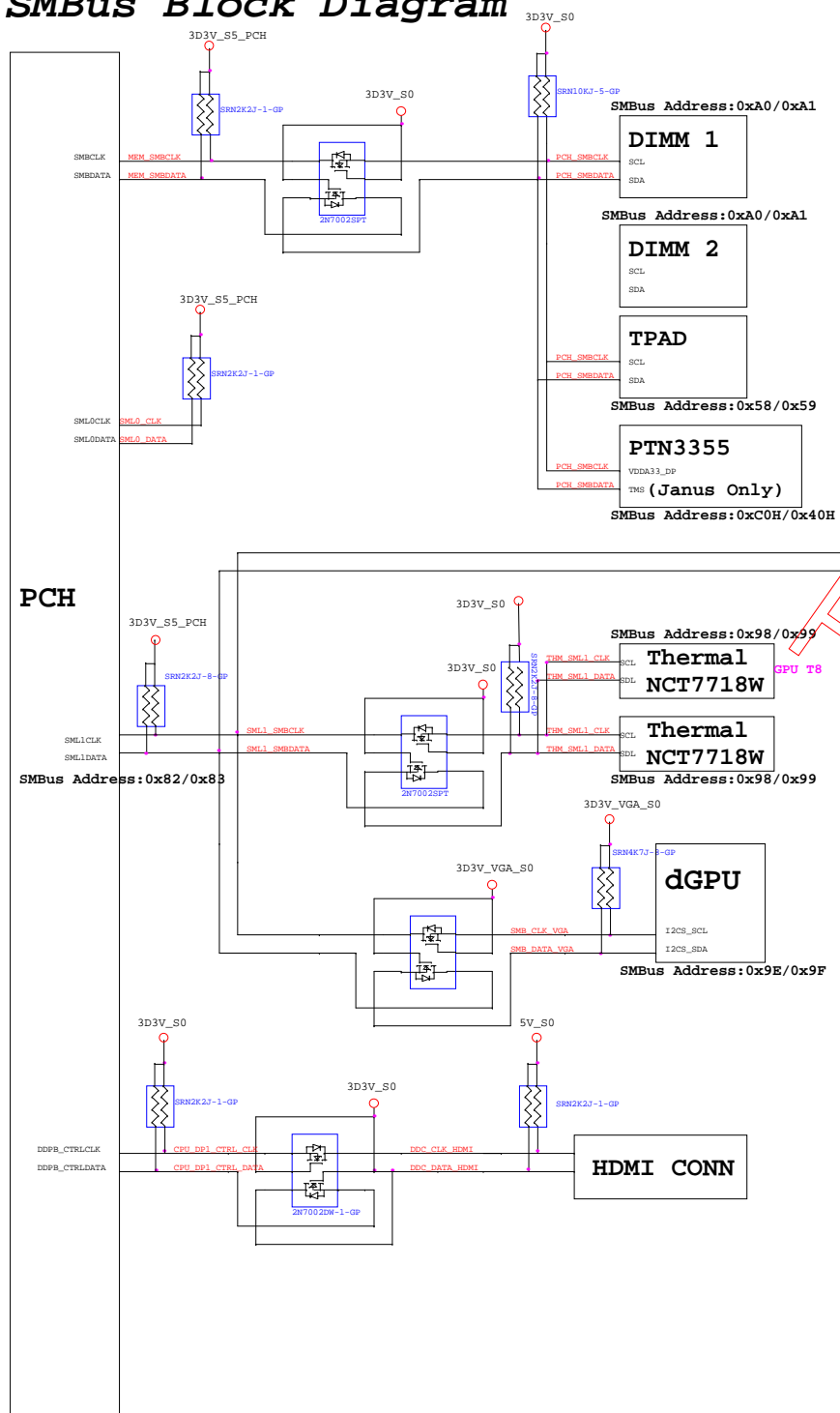
CLK Block Diagram



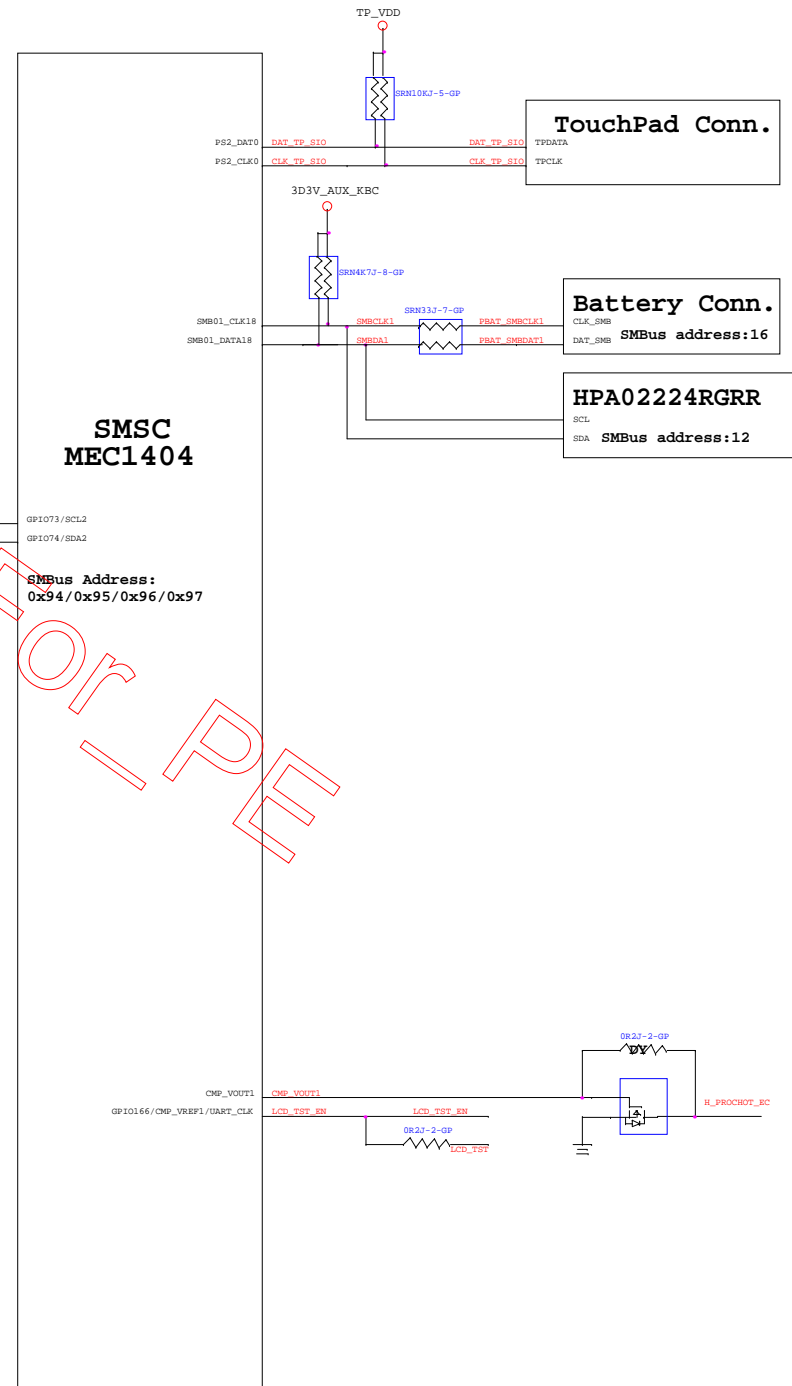
[illegible]

FORM

PCH SMBus Block Diagram

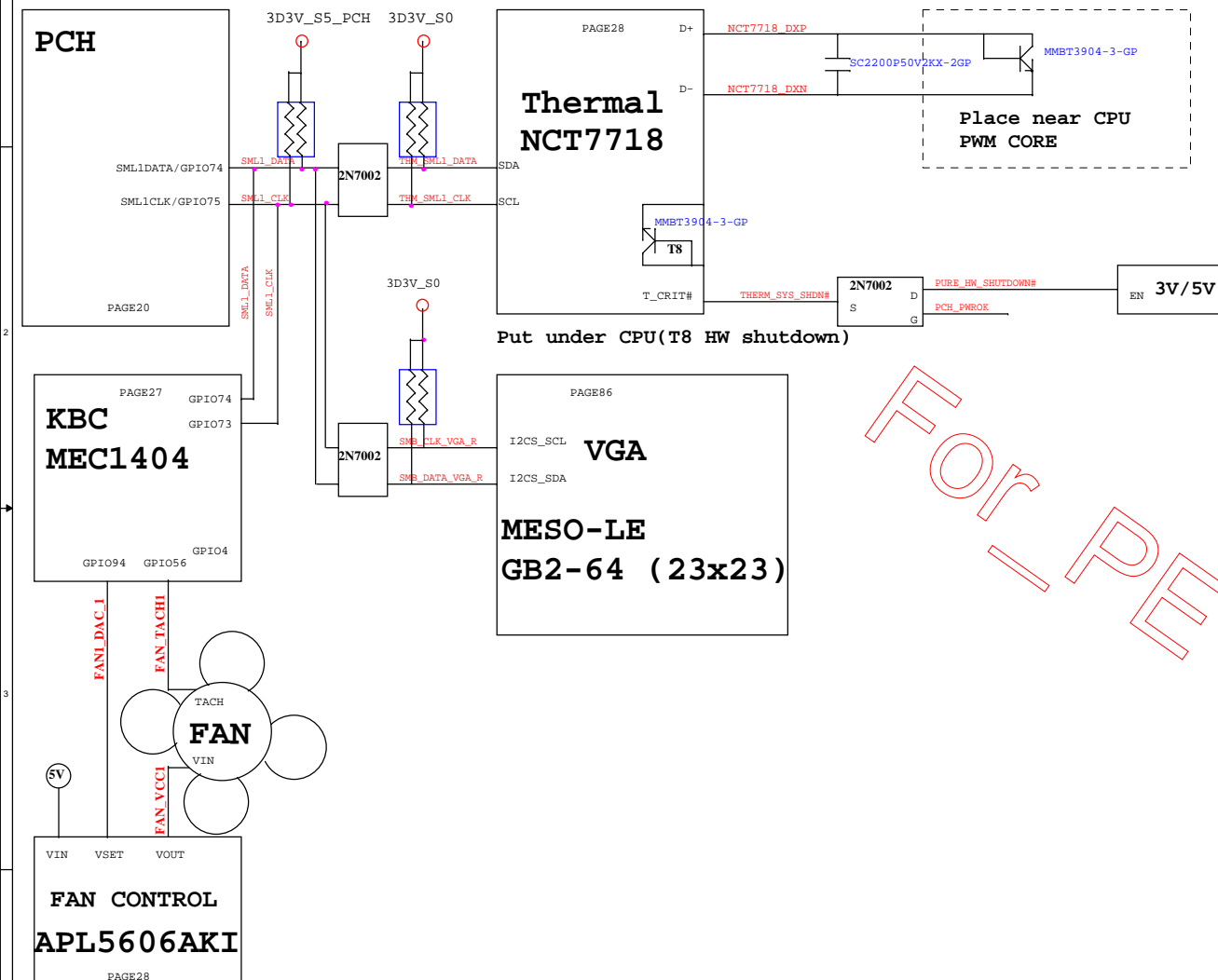


KBC SMBus Block Diagram



<Core Design>

Thermal Block Diagram



Audio Block Diagram

